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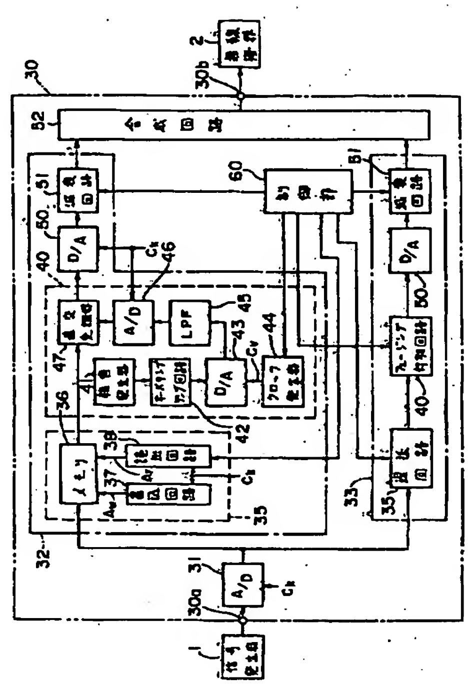
(54)【発明の名称】　フェージングシミュレータ

(57)【要約】

【課題】　フェージングを変化させるときの信号瞬断がなく、正確に遅延された信号を出力できるようにする。

【解決手段】　A／D変換器31によってディジタル信号に変換した所定信号をメモリ36にアドレス順に記憶し、これを順次読み出すとともに、書込アドレスに対する読出アドレスの差を可変して信号の遅延時間を可変する。また、DSPによる雑音発生器41から出力された雑音信号をオーバサンプリング処理してからD／A変換してアナログ信号に変換し、この信号から低域通過フィルタ45によってイメージ成分を除去して直交変調器47へ入力して、遅延回路35から出力された信号に対してフェージング変動とドップラシフトを与え、D／A変換器43に対するクロック周波数を可変して雑音信号の帯域を可変してフェージング変動量とドップラシフト量を変動させる。



【特許請求の範囲】

【請求項１】入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、

前記所定信号をディジタル信号に変換するＡ／Ｄ変換器（３１）を有し、

前記遅延回路が、

書込アドレスと読出アドレスとを独立に指定できるメモリ（３６）と、

前記メモリに対する書込アドレスを所定順に指定して、前記Ａ／Ｄ変換器から出力されたディジタル信号を前記メモリに記憶させる書込手段（３７）と、

前記メモリに対する読出アドレスを順次指定して前記メモリに記憶されたディジタル信号を読み出し前記フェージング付加回路へ送出する読出手段（３８）と、

前記読出手段が前記メモリに指定する読出アドレスを可変制御して、前記メモリに記憶されたディジタル信号が読み出されるまでの遅延時間を任意に可変する制御手段（６０）とを備えたことを特徴とするフェージングシミュレータ。

【請求項２】入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、

前記フェージング付加回路が、

ディジタルの雑音信号を発生する雑音発生器（４１）と、

前記雑音信号をオーバサンプリング処理して、雑音信号のイメージ成分を高域側へシフトするオーバサンプリング手段（４２）と、

クロック信号を出力する周波数可変のクロック発生器（４４）と、

前記オーバサンプリング処理された雑音信号を前記クロック発生器からのクロック信号に同期してアナログ信号に変換するＤ／Ａ変換器（４３）と、

前記Ｄ／Ａ変換器によってアナログ信号に変換された雑音信号から前記イメージ成分を除去する低域通過フィルタ（４５）と、

前記低域通過フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、

前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えたことを特徴とするフェージングシミュレータ。

【請求項３】前記減衰回路は、前記オーバサンプリング手段の出力信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする請求項２記載のフェージングシミュレータ。

【請求項４】入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、

前記フェージング付加回路が、

ディジタルの雑音信号を発生する雑音発生器（４１）と、

クロック信号を出力する周波数可変のクロック発生器（４４）と、

前記クロック発生器からのクロック信号に同期して前記雑音信号をアナログ信号に変換するＤ／Ａ変換器（４３）と、

前記クロック発生器からのクロック信号の周波数に応じて高域遮断周波数が変化し、前記Ｄ／Ａ変換器から出力された雑音信号に含まれるイメージ成分を除去する帯域可変フィルタ（７１）と、

前記帯域可変フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、

前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えたことを特徴とするフェージングシミュレータ。

【請求項５】前記減衰回路が、前記雑音発生器から出力された雑音信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする請求項４記載のフェージングシミュレータ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、所定信号に対して遅延処理、フェージング付加処理および減衰処理を行い、これらの処理を行なった信号を、伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、遅延特性やフェージング特性を変化させる際に、信号の瞬断を発生させないようにするための技術に関する。

【０００２】

【従来の技術】電波によって通信を行なうシステムでは、数々の伝搬路を想定して、端末機、基地局あるいは

それらを試験するための試験機器等の無線機器の動作をチェックする必要がある。

【０００３】特に、移動局の場合、伝搬路の伝搬特性が時間とともに大きく変動する。この伝搬特性の変動の要素は、マルチパスの伝搬時間差、フェージング変動、ドップラシフト変動および遮蔽物等による減衰変動であり、無線機器の動作をチェックするためには、所定信号に遅延処理、フェージング付加処理および減衰処理を行い、これらの処理を行なった信号を、模擬伝搬信号として無線機器に与える必要がある。

【０００４】図６は、このような目的で一般的に用いられているマルチパス型のフェージングシミュレータ１０の構成を示している。

【０００５】このフェージングシミュレータ１０は、信号発生器１から出力された所定信号（通信に使用される安定なアナログの信号）を入力端子１０ａを介して受け、これを分岐して、２つの伝搬路模擬回路１１、１２に入力する。

【０００６】伝搬路模擬回路１１、１２は、所定信号を遅延する遅延回路１３、遅延回路１３から出力された信号にフェージング変動とドップラシフトを与えるフェージング付加回路１７、フェージング付加回路１７から出力された信号に減衰を与える減衰回路２１によって構成されている。

【０００７】遅延回路１３は、入力信号をディジタル信号に変換するＡ／Ｄ変換器１４と、Ａ／Ｄ変換器１４の出力を受け一定の遅延を発生させるシフトレジスタ１５と、シフトレジスタ１５からの出力をアナログ信号に変換するＤ／Ａ変換器１６とによって構成されており、図示しない制御部からの制御信号によってシフトレジスタ１５の段数を可変させることにより所定信号に対する遅延時間を変化させる。

【０００８】フェージング付加回路１７は、雑音発生器１８、Ｄ／Ａ変換器１９および直交変調器２０によって構成されており、雑音発生器１８から出力されるディジタルの白色雑音信号をＤ／Ａ変換器１９によってアナログの雑音信号に変換して直交変調器２０に出力する。

【０００９】直交変調器２０は、Ｄ／Ａ変換器１９から出力された雑音信号によって、所定信号の振幅および位相を変調してフェージング変動およびドップラシフトを施す。

【００１０】このフェージング付加回路１７は、制御部からの制御信号によって雑音発生器１８のプログラムを変更することにより、所定信号に対するフェージング変動量やドップラシフト量を変化させる。

【００１１】また、減衰回路２１は、制御部からの制御信号によってフェージング付加回路１７から出力された信号に対する減衰量を変化させる。

【００１２】このように構成された２つの伝搬路模擬回路１１、１２の出力は、あたかも同一送信機から発射され２つの異なる伝搬路を経た電波と同等であり、その両出力を合成回路２２によって合成した合成信号を出力端子１０ｂから評価対象の無線機器２に入力することによって、無線機器２の動作を実際の使用状態でチェックすることができる。

【００１３】

【発明が解決しようとする課題】しかしながら、前記した従来のフェージングシミュレータでは、フェージング変動量等を変更するたびに雑音発生器のプログラムを変更しなければならず、プログラム変更の間に信号の瞬断が発生してしまう。

【００１４】また、前記した遅延回路のようにシフトレジスタの段数を変えて遅延時間を可変する方法では、遅延時間変更のためにシフトレジスタの段数を変更しても直ちに意図した遅延信号が出力されないことがあり、無線機器の動作チェックに支障がある。

【００１５】本発明は、これらの問題を解決したフェージングシミュレータを提供することを目的としている。

【００１６】

【課題を解決するための手段】前記目的を達成するために、本発明の請求項１のフェージングシミュレータは、入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、前記所定信号をディジタル信号に変換するＡ／Ｄ変換器（３１）を有し、前記遅延回路が、書込アドレスと読出アドレスとを独立に指定できるメモリ（３６）と、前記メモリに対する書込アドレスを所定順に指定して、前記Ａ／Ｄ変換器から出力されたディジタル信号を前記メモリに記憶させる書込手段（３７）と、前記メモリに対する読出アドレスを順次指定して前記メモリに記憶されたディジタル信号を読み出し前記フェージング付加回路へ送出する読出手段（３８）と、前記読出手段が前記メモリに指定する読出アドレスを可変制御して、前記メモリに記憶されたディジタル信号が読み出されるまでの遅延時間を任意に可変する制御手段（６０）とを備えている。

【００１７】また、本発明の請求項２のフェージングシミュレータは、入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、前記フェージング付加回路が、ディジタルの雑音信号を発生する雑音発生器（４１）と、前記雑音信号をオーバサンプリング処理して、

雑音信号のイメージ成分を高域側へシフトするオーバサンプリング手段（４２）と、クロック信号を出力する周波数可変のクロック発生器（４４）と、前記オーバサンプリング処理された雑音信号を前記クロック発生器からのクロック信号に同期してアナログ信号に変換するＤ／Ａ変換器（４３）と、前記Ｄ／Ａ変換器によってアナログ信号に変換された雑音信号から前記イメージ成分を除去する低域通過フィルタ（４５）と、前記低域通過フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えている。

【００１８】また、本発明の請求項３のフェージングシミュレータは、請求項２記載のフェージングシミュレータにおいて、前記減衰回路は、前記オーバサンプリング手段の出力信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする。

【００１９】また、本発明の請求項４のフェージングシミュレータは、入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、前記フェージング付加回路が、ディジタルの雑音信号を発生する雑音発生器（４１）と、クロック信号を出力する周波数可変のクロック発生器（４４）と、前記クロック発生器からのクロック信号に同期して前記雑音信号をアナログ信号に変換するＤ／Ａ変換器（４３）と、前記クロック発生器からのクロック信号の周波数に応じて高域遮断周波数が変化し、前記Ｄ／Ａ変換器から出力された雑音信号に含まれるイメージ成分を除去する帯域可変フィルタ（７１）と、前記帯域可変フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えている。

【００２０】また、本発明の請求項５のフェージングシミュレータは、請求項４記載のフェージングシミュレータにおいて、前記減衰回路が、前記雑音発生器から出力された雑音信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする。

【００２１】

【発明の実施の形態】以下、図面に基づいて本発明の一実施形態を説明する。図１は、本発明の一実施形態の２パス型のフェージングシミュレータ３０の構成を示している。

【００２２】なお、本発明は１パス型のフェージングシミュレータでも動作する。２パス型の場合には、例えば局間の直接の伝搬ルートと反射波のルートの２ルートの試験が可能であるのに対し、１パス型の場合には、直接の伝搬ルートだけの試験となる。２パス型としては反射波と別の反射波の２伝搬ルートを試験することもできる。また、３パス、４パス、…とパスを増して試験することもできる。いずれも原理は同じなので、ここでは２パス型で説明する。

【００２３】図１において、信号発生器１から出力される所定信号は、フェージングシミュレータ３０の入力端子３０ａを介してＡ／Ｄ変換器３１に入力される。

【００２４】Ａ／Ｄ変換器３１は、所定信号をクロック信号Ｃｋに同期する周期でサンプリングしてディジタル信号に変換する。

【００２５】Ａ／Ｄ変換器３１によってディジタル信号に変換された所定信号は分岐されて２つの伝搬路模擬回路３２、３３へ入力される。

【００２６】伝搬路模擬回路３２、３３は同一構成であり、それぞれ遅延回路３５、フェージング付加回路４０、Ｄ／Ａ変換器５０および減衰回路５１によって構成されている。

【００２７】遅延回路３５は、後述する制御部６０とともにこの実施形態の遅延回路を構成するものであり、メモリ３６、書込回路３７および読出回路３８によって構成されている。メモリ３６は書込アドレスと読出アドレスとを独立に指定でき、独立した入出力ポートを有するデュアルポートＲＡＭによって形成されている。

【００２８】書込回路３７は、メモリ３６に対する書込アドレスＡｗをクロック信号Ｃｋに同期して所定順に指定して、Ａ／Ｄ変換器３１から出力されたディジタル信号をメモリ３６に記憶させる。

【００２９】読出回路３８は、メモリに対する読出アドレスＡｒをクロック信号Ｃｋに同期して順次指定してメモリ３６に記憶されたディジタル信号を読み出す。

【００３０】したがって、メモリ３６に書き込まれたディジタル信号は、書込アドレスＡｗと読出アドレスＡｒとの差ΔＡにクロック信号Ｃｋの周期を乗じた時間だけ遅れて読み出される。なお、読出回路３８は、後述する制御部６０からの遅延制御信号に応じて、ΔＡが変化するように読出アドレスＡｒを可変する。

【００３１】フェージング付加回路４０は、後述する制御部６０とともにこの実施形態のフェージング付加回路を構成するものであり、ＤＳＰによって構成された雑音発生器４１から出力されるディジタルの白色雑音信号をオーバサンプリング回路４２に入力する。

【００３２】オーバサンプリング回路４２は、例えば雑

音発生器４１から出力された雑音信号系列が〔N_1，N_2，…，N_k，…　〕であれば、これを〔N_1，０，…，０，N_2，０，…，０，…，N_k，０，…，０，…〕のように、各信号間を複数（Ｍ－１）個の０データで補間し、これをディジタルフィルタに通過させることにより、雑音信号の信号成分自体を変化させずにイメージ成分のみを高域にシフトする。このように、信号間をＭ－１個の０データで補間してフィルタリングする方式をＭ倍オーバサンプリングという。

【００３３】さらに詳しく説明すると、雑音発生器４１から出力された雑音信号をオーバサンプリング処理をせずにクロック発生器４４の周波数ｆｓの速度でＤ／Ａ変換した場合、図２に示すように、雑音信号の基本成分Ｒに対して最も周波数が近いイメージ成分I_1が周波数ｆｓを中心に発生する。したがって、このイメージ成分I_1を除去するための低域通過フィルタが必要となる。

【００３４】この低域通過フィルタの高域遮断周波数ｆａは、通常、図２の特性Ｆのように、周波数ｆｓのほぼ１／２に設定されるため、周波数ｆｓの最大値をｆｓｍとすると、周波数がｆｓｍ時の雑音信号の基本成分Ｒの帯域およびフィルタの高域遮断周波数ｆａをｆｓｍ／２に設定した場合、周波数ｆｓを可変させ基本成分Ｒの帯域を狭くすると、イメージ成分I_1が低域通過フィルタを通過してしまう。

【００３５】これに対し、この実施形態のように雑音発生器４１から出力された雑音信号に対してＭ倍オーバサンプリング処理を行うと、図２に示しているように、雑音信号の基本成分Ｒに対して最も周波数が近いイメージ成分I_2が周波数Ｍ・ｆｓを中心に発生する。これにより、後述する低域通過フィルタ４５の高域遮断周波数を固定した状態でも、周波数ｆｓを可変させることにより雑音信号の基本成分Ｒの帯域をほぼｆａ／２からｆｓｍ／２にわたって可変させることができる。

【００３６】このようにしてオーバサンプリング処理された雑音信号は、Ｄ／Ａ変換器４３によってアナログ信号に変換される。Ｄ／Ａ変換器４３は、クロック発生器４４からのクロック信号Ｃｖに同期して雑音信号をアナログ信号に変換して、低域通過フィルタ４５へ出力する。

【００３７】クロック発生器４４は、後述する制御部６０からの雑音制御信号に応じてクロック信号Ｃｖの周波数を可変して、雑音信号の基本成分の帯域を可変させ、雑音信号の波形を変化させる。

【００３８】低域通過フィルタ４５の出力信号は、Ａ／Ｄ変換器４６によってディジタル信号に変換され直交変調器４７に出力される。なお、Ａ／Ｄ変換器４６はクロック信号Ｃｋに同期してディジタル変換を行なう。

【００３９】直交変調器４７は、遅延回路３５のメモリ３６から読み出されたディジタル信号をＡ／Ｄ変換器４６から出力されたディジタルの雑音信号によって変調して、フェージング変動およびドップラシフトを付加する。

【００４０】直交変調器４７から出力された信号は、Ｄ／Ａ変換器５０によってアナログ信号に変換され、減衰回路５１に入力される。

【００４１】減衰回路５１は、制御部６０からの減衰制御信号に応じて直交変調器４７から出力された信号に対する減衰量を変化させる。

【００４２】伝搬路模擬回路３２、３３の各減衰回路５１から出力された信号は、合成回路５２に入力されて合成され、その合成信号が出力端子３０ｂから評価対象の無線機器２へ出力される。

【００４３】制御部６０は、伝搬路模擬回路３２、３３の遅延回路３５、フェージング付加回路４０および減衰回路５１に対する遅延制御信号、雑音制御信号および減衰制御信号を、予め設定された変動パターンにしたがって連続的に変化させ、例えば、評価対象の無線機器２が移動局の場合には基地局からの電波を移動しながら受信したときの受信信号と同様に変動する合成信号を無線機器２に出力する。

【００４４】このように、実施形態のフェージングシミュレータ３０の遅延処理は、Ａ／Ｄ変換器３１によってディジタル信号に変換された所定信号を、書込アドレスと読出アドレスとを独立に指定できるメモリ３６にアドレス順に記憶し、これをアドレス差のある状態で順次読み出すとともに、書込アドレスに対する読出アドレスの差を可変して信号の遅延時間を可変している。

【００４５】このため、遅延時間を変動する際に直ちに、アドレスの差に対応した正確な遅延時間を与えることができる。

【００４６】また、フェージングシミュレータ３０のフェージング付加処理は、ＤＳＰによる雑音発生器４１から出力された一定のサンプリングレートに対して帯域固定の雑音信号をオーバサンプリング処理してから、Ｄ／Ａ変換してアナログ信号に変換し、この信号から周波数固定の低域通過フィルタ４５によってイメージ成分を除去して直交変調器４７へ入力して、遅延回路３５から出力された信号に対してフェージング変動とドップラシフトを与え、Ｄ／Ａ変換器４３に対するクロック周波数を可変して雑音信号の帯域を可変してフェージング変動量とドップラシフト量を変動させている。

【００４７】このため、精度の高い雑音信号が得られ、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、ＤＳＰのプログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【００４８】

【他の実施の形態】前記実施形態のフェージング付加処理では、雑音信号に対してオーバサンプリング処理を行なうことによって、Ｄ／Ａ変換時に発生する雑音信号の

イメージ周波数を高域側にシフトして、周波数固定の低域通過フィルタでそのイメージ周波数を除去していたが、図３に示すフェージング付加回路７０のように、雑音発生器４１から出力された雑音信号をＤ／Ａ変換器４３によってアナログの雑音信号に変換し、この雑音信号に含まれるイメージ成分をスイッチトキャパシタフィルタ（以下、ＳＣＦと記す）７１によって除去するようにしてもよい。

【００４９】なお、ＳＣＦ７１の後段に設けられている低域通過フィルタ（ＬＰＦ）７２は、ＳＣＦ７１の出力からクロック信号Ｃｖ成分を除去するためのものである。

【００５０】ＳＣＦ７１は、クロック信号Ｃｖの周波数に応じた遮断周波数で入力信号に対する帯域制限を行なう帯域可変フィルタ素子であり、低域通過フィルタとして用いた場合、クロック信号Ｃｖの周波数が高くなるとそれに応じて高域遮断周波数が高い方へシフトする。

【００５１】したがって、あるクロック周波数において図４の（ａ）の特性Ｇのように、ＳＣＦ７１の高域遮断周波数ｆｂを雑音信号の基本成分Ｒの帯域より僅かに高い周波数に設定しておけば、図４の（ｂ）のようにクロック信号Ｃｖの周波数を可変したとき、ＳＣＦ７１の高域遮断周波数ｆｂも同一方向に変化し、雑音信号のイメージ成分Ｉを除去してその基本成分Ｒのみを通過させることができ、信号に対する瞬断を発生させることなく、フェージング変動量およびドップラシフト量を変化させることができる。

【００５２】なお、ここでは、ＳＣＦ７１を帯域可変フィルタとして用いているが、Ｄ／Ａ変換器４３のクロック信号の周波数に応じて高域遮断周波数を可変できるものであれば、他の帯域可変フィルタを用いることもできる。

【００５３】また、前記実施形態では、２つの伝搬路模擬回路を有する２パス型のフェージングシミュレータに本発明を適用していたが、本発明は、３パス以上のフェージングシミュレータや、伝搬路模擬回路が１つだけの１パス型のフェージングシミュレータにも同様に適用できる。

【００５４】また、前記実施形態では、遅延処理およびフェージング付加処理が成された信号に対して減衰処理を直接行なうようにしていたが、例えば、図５に示すように、雑音発生器４１から出力された雑音信号をオーバサンプリング回路４２によってオーバサンプリング処理し、オーバサンプリング処理された雑音信号をディジタル型の減衰回路７６に入力して減衰処理を行い、減衰処理した信号をＤ／Ａ変換器４３によってアナログ信号に変換するように構成してもよい。

【００５５】なお、減衰回路７６を雑音発生器４１とオーバサンプリング回路４２の間に設けた場合には、減衰回路がＤ／Ａ変換器４３のクロックに同期して動作してしまうが、図５のように、減衰回路７６をオーバサンプリング回路４２とＤ／Ａ変換器４３の間に設けた場合には、減衰制御とＤ／Ａ変換器４３のクロックの可変制御とを独立に行なえ、減衰処理を遅延なく行なうことができる。

【００５６】なお、図５のようにフェージング付加回路内に減衰回路を設けた場合には、Ｄ／Ａ変換器５０の出力を合成回路５２によって合成して無線機器２へ与える。

【００５７】

【発明の効果】以上説明したように、本発明の請求項１のフェージングシミュレータでは、Ａ／Ｄ変換器によってディジタル信号に変換された所定信号を、書込アドレスと読出アドレスとを独立に指定できるメモリにアドレス順に記憶し、これをアドレス差のある状態で順次読み出すとともに、書込アドレスに対する読出アドレスの差を可変して信号の遅延時間を可変している。

【００５８】このため、遅延時間を変動する際に直ちにアドレスの差に対応した正確な遅延時間を与えることができる。

【００５９】また、本発明の請求項２のフェージングシミュレータでは、雑音発生器から出力されたディジタルの雑音信号をオーバサンプリング処理してから、Ｄ／Ａ変換してアナログ信号に変換し、この信号から周波数固定の低域通過フィルタによってイメージ成分を除去し、このイメージ成分を除去した雑音信号によって所定信号を変調するとともに、Ｄ／Ａ変換器に対するクロック周波数を可変して雑音信号の帯域を可変して、所定信号にフェージング変動とドップラシフトを与えている。

【００６０】このため、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、プログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【００６１】また、本発明の請求項４のフェージングシミュレータでは、雑音発生器から出力されたディジタルの雑音信号をＤ／Ａ変換してアナログ信号に変換し、この信号から帯域可変フィルタによってイメージ成分を除去し、このイメージ成分を除去した雑音信号によって所定信号を変調するとともに、Ｄ／Ａ変換器に対するクロック周波数を可変して雑音信号の帯域を可変して、所定信号にフェージング変動とドップラシフトを与えている。

【００６２】このため、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、プログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【図面の簡単な説明】

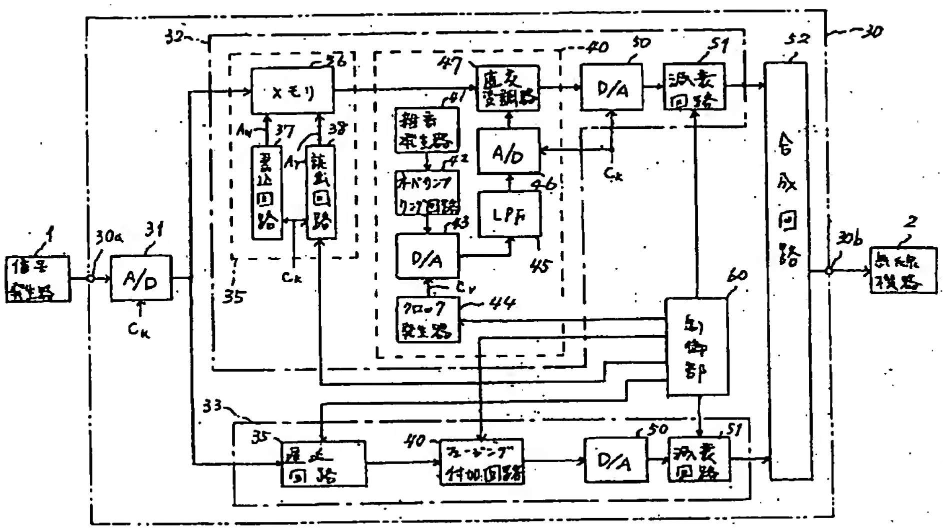
【図１】本発明の一実施形態の構成を示すブロック図

【図２】一実施形態の動作を説明するための図

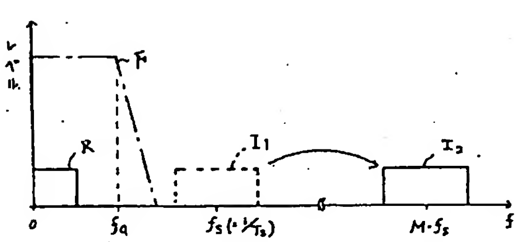
【図３】本発明の他の実施形態の構成を示すブロック図

【図４】他の実施形態の動作を説明するための図
【図５】本発明の他の実施形態の構成を示すブロック図
【図６】従来装置の構成を示すブロック図
【符号の説明】
３０　フェージングシミュレータ
３１　Ａ／Ｄ変換器
３２、３３　伝搬路模擬回路
３５　遅延回路
３６　メモリ
３７　書込回路
３８　読出回路
４０　フェージング付加回路
＊４１　雑音発生器
４２　オーバサンプリング回路
４３　Ｄ／Ａ変換器
４４　クロック発生器
４５　低域通過フィルタ
４６　Ａ／Ｄ変換器
４７　直交変調器
５０　Ｄ／Ａ変換器
５１　減衰回路
５２　合成回路
６０　制御部
＊

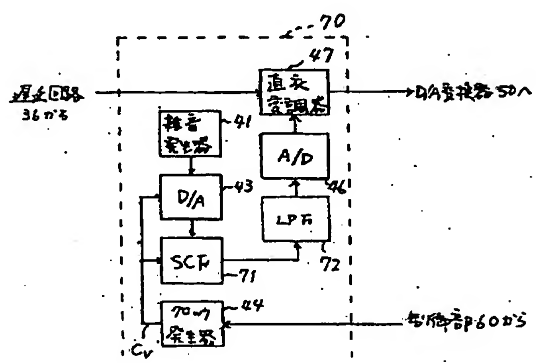
【図１】



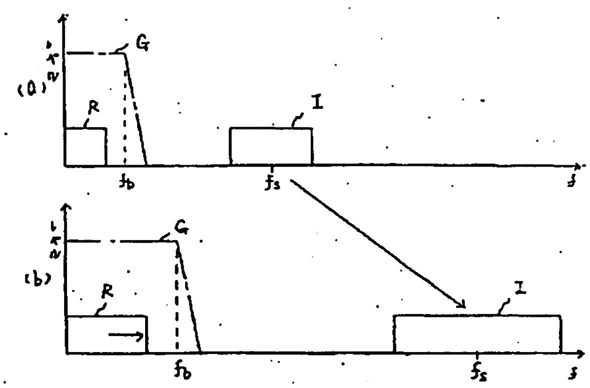
【図２】



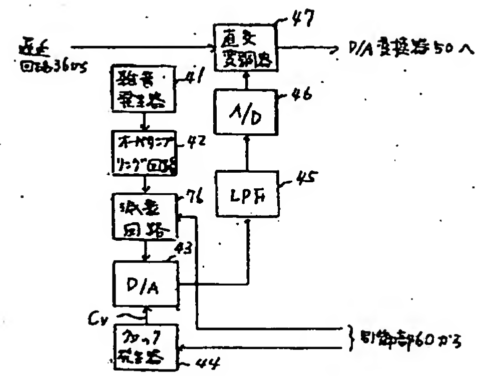
【図３】



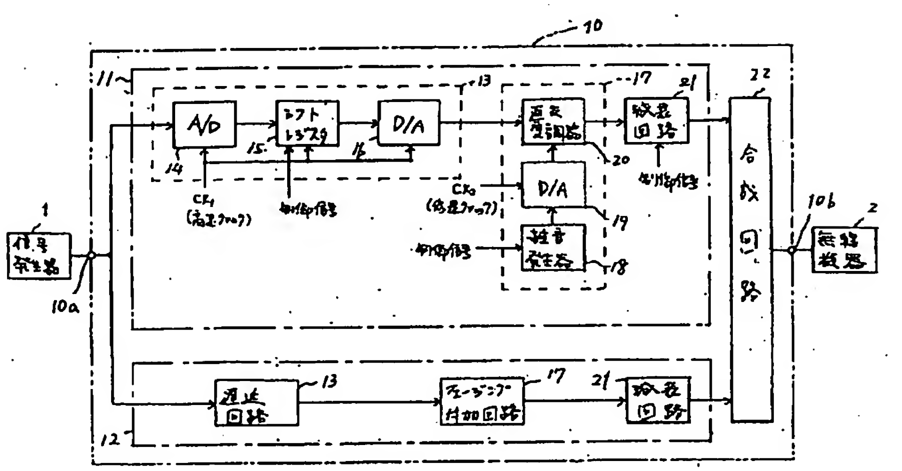
【図４】



【図５】

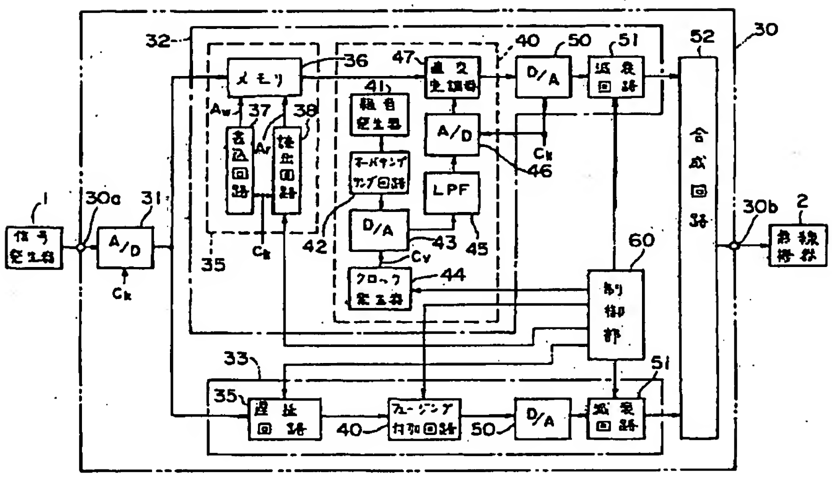


【図６】

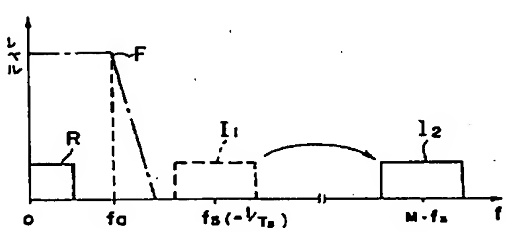


【手続補正書】
【提出日】平成１０年４月３０日
【手続補正１】
【補正対象書類名】図面
【補正対象項目名】全図
【補正方法】変更
【補正内容】

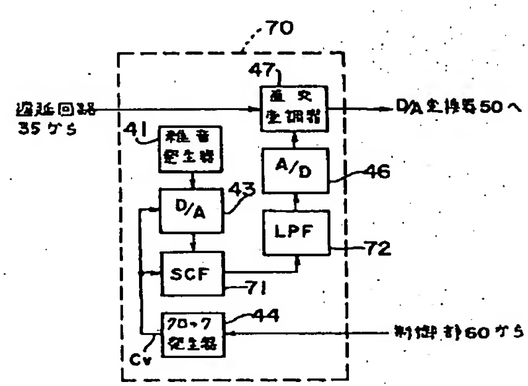
【図1】



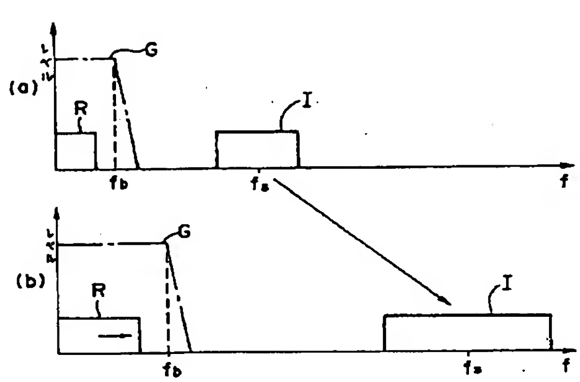
【図2】



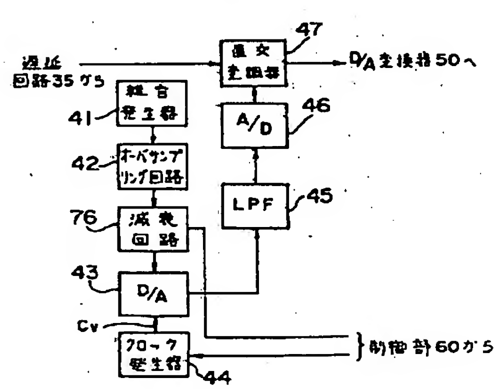
【図3】



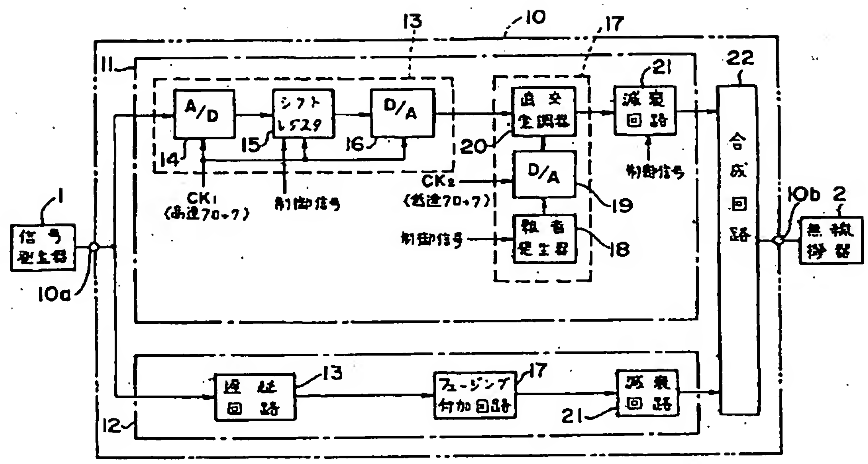
【図4】



【図5】



【図６】



【手続補正書】
【提出日】平成１１年７月９日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】全文
【補正方法】変更
【補正内容】
【書類名】　明細書
【発明の名称】　フェージングシミュレータ
【特許請求の範囲】
【請求項１】入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、
前記フェージング付加回路が、
ディジタルの雑音信号を発生する雑音発生器（４１）と、
前記雑音信号をオーバサンプリング処理して、雑音信号のイメージ成分を高域側へシフトするオーバサンプリング手段（４２）と、
クロック信号を出力する周波数可変のクロック発生器（４４）と、
前記オーバサンプリング処理された雑音信号を前記クロック発生器からのクロック信号に同期してアナログ信号に変換するＤ／Ａ変換器（４３）と、
前記Ｄ／Ａ変換器によってアナログ信号に変換された雑音信号から前記イメージ成分を除去する低域通過フィルタ（４５）と、
前記低域通過フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、
前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えたことを特徴とするフェージングシミュレータ。
【請求項２】前記減衰回路は、前記オーバサンプリング手段の出力信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする請求項１記載のフェージングシミュレータ。
【請求項３】入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、
前記フェージング付加回路が、
ディジタルの雑音信号を発生する雑音発生器（４１）と、
クロック信号を出力する周波数可変のクロック発生器（４４）と、
前記クロック発生器からのクロック信号に同期して前記雑音信号をアナログ信号に変換するＤ／Ａ変換器（４３）と、
前記クロック発生器からのクロック信号の周波数に応じ

て高域遮断周波数が変化し、前記D／A変換器から出力された雑音信号に含まれるイメージ成分を除去する帯域可変フィルタ（７１）と、
前記帯域可変フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、
前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えたことを特徴とするフェージングシミュレータ。
【請求項４】前記減衰回路が、前記雑音発生器から出力された雑音信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする請求項３記載のフェージングシミュレータ。
【請求項５】前記所定信号をディジタル信号に変換するA／D変換器（３１）を有し、
前記遅延回路が、
書込アドレスと読出アドレスとを独立に指定できるメモリ（３６）と、
前記メモリに対する書込アドレスを所定順に指定して、前記A／D変換器から出力されたディジタル信号を前記メモリに記憶させる書込手段（３７）と、
前記メモリに対する読出アドレスを順次指定して前記メモリに記憶されたディジタル信号を読み出し前記フェージング付加回路へ送出する読出手段（３８）とを備え、
前記制御手段は、
前記読出手段が前記メモリに指定する読出アドレスを可変制御して、前記メモリに記憶されたディジタル信号が読み出されるまでの遅延時間を任意に可変することを特徴とする請求項１または請求項２または請求項３または請求項４記載のフェージングシミュレータ。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、所定信号に対して遅延処理、フェージング付加処理および減衰処理を行い、これらの処理を行なった信号を、伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、遅延特性やフェージング特性を変化させる際に、信号の瞬断を発生させないようにするための技術に関する。
【０００２】
【従来の技術】電波によって通信を行なうシステムでは、数々の伝搬路を想定して、端末機、基地局あるいはそれらを試験するための試験機器等の無線機器の動作をチェックする必要がある。
【０００３】特に、移動局の場合、伝搬路の伝搬特性が時間とともに大きく変動する。この伝搬特性の変動の要素は、マルチパスの伝搬時間差、フェージング変動、ドップラシフト変動および遮蔽物等による減衰変動であり、無線機器の動作をチェックするためには、所定信号に遅延処理、フェージング付加処理および減衰処理を行い、これらの処理を行なった信号を、模擬伝搬信号として無線機器に与える必要がある。
【０００４】図６は、このような目的で一般的に用いられているマルチパス型のフェージングシミュレータ１０の構成を示している。
【０００５】このフェージングシミュレータ１０は、信号発生器１から出力された所定信号（通信に使用される安定なアナログの信号）を入力端子１０ａを介して受け、これを分岐して、２つの伝搬路模擬回路１１、１２に入力する。
【０００６】伝搬路模擬回路１１、１２は、所定信号を遅延する遅延回路１３、遅延回路１３から出力された信号にフェージング変動とドップラシフトを与えるフェージング付加回路１７、フェージング付加回路１７から出力された信号に減衰を与える減衰回路２１によって構成されている。
【０００７】遅延回路１３は、入力信号をディジタル信号に変換するA／D変換器１４と、A／D変換器１４の出力を受け一定の遅延を発生させるシフトレジスタ１５と、シフトレジスタ１５からの出力をアナログ信号に変換するD／A変換器１６とによって構成されており、図示しない制御部からの制御信号によってシフトレジスタ１５の段数を可変させることにより所定信号に対する遅延時間を変化させる。
【０００８】フェージング付加回路１７は、雑音発生器１８、D／A変換器１９および直交変調器２０によって構成されており、雑音発生器１８から出力されるディジタルの白色雑音信号をD／A変換器１９によってアナログの雑音信号に変換して直交変調器２０に出力する。
【０００９】直交変調器２０は、D／A変換器１９から出力された雑音信号によって、所定信号の振幅および位相を変調してフェージング変動およびドップラシフトを施す。
【００１０】このフェージング付加回路１７は、制御部からの制御信号によって雑音発生器１８のプログラムを変更することにより、所定信号に対するフェージング変動量やドップラシフト量を変化させる。
【００１１】また、減衰回路２１は、制御部からの制御信号によってフェージング付加回路１７から出力された信号に対する減衰量を変化させる。
【００１２】このように構成された２つの伝搬路模擬回路１１、１２の出力は、あたかも同一送信機から発射され２つの異なる伝搬路を経た電波と同等であり、その両出力を合成回路２２によって合成した合成信号を出力端子１０ｂから評価対象の無線機器２に入力することによって、無線機器２の動作を実際の使用状態でチェックすることができる。
【００１３】

【発明が解決しようとする課題】しかしながら、前記した従来のフェージングシミュレータでは、フェージング変動量等を変更するたびに雑音発生器のプログラムを変更しなければならず、プログラム変更の間に信号の瞬断が発生してしまう。

【０００１４】また、前記した遅延回路のようにシフトレジスタの段数を変えて遅延時間を可変する方法では、遅延時間変更のためにシフトレジスタの段数を変更しても直ちに意図した遅延信号が出力されないことがあり、無線機器の動作チェックに支障がある。

【００１５】本発明は、これらの問題を解決したフェージングシミュレータを提供することを目的としている。

【００１６】

【課題を解決するための手段】前記目的を達成するために、本発明の請求項１のフェージングシミュレータは、入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、前記フェージング付加回路が、ディジタルの雑音信号を発生する雑音発生器（４１）と、前記雑音信号をオーバサンプリング処理して、雑音信号のイメージ成分を高域側へシフトするオーバサンプリング手段（４２）と、クロック信号を出力する周波数可変のクロック発生器（４４）と、前記オーバサンプリング処理された雑音信号を前記クロック発生器からのクロック信号に同期してアナログ信号に変換するＤ／Ａ変換器（４３）と、前記Ｄ／Ａ変換器によってアナログ信号に変換された雑音信号から前記イメージ成分を除去する低域通過フィルタ（４５）と、前記低域通過フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えている。

【００１７】また、本発明の請求項２のフェージングシミュレータは、請求項１記載のフェージングシミュレータにおいて、前記減衰回路は、前記オーバサンプリング手段の出力信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする。

【００１８】また、本発明の請求項３のフェージングシミュレータは、入力された所定信号に対して遅延処理を行う遅延回路と、前記遅延回路の出力を受けてフェージング変動を付加するフェージング付加回路と、前記フェージング付加回路の出力を減衰処理する減衰回路とを有し、これらの各処理を行った信号を伝搬特性が変化する伝搬路を伝搬した模擬伝搬信号として出力するフェージングシミュレータにおいて、前記フェージング付加回路が、ディジタルの雑音信号を発生する雑音発生器（４１）と、クロック信号を出力する周波数可変のクロック発生器（４４）と、前記クロック発生器からのクロック信号に同期して前記雑音信号をアナログ信号に変換するＤ／Ａ変換器（４３）と、前記クロック発生器からのクロック信号の周波数に応じて高域遮断周波数が変化し、前記Ｄ／Ａ変換器から出力された雑音信号に含まれるイメージ成分を除去する帯域可変フィルタ（７１）と、前記帯域可変フィルタの出力信号によって前記遅延回路の出力信号を変調して、フェージング変動とドップラシフトを与える変調器（４７）と、前記クロック発生器のクロック周波数を可変制御して、前記遅延回路の出力信号に対するフェージング変動量とドップラシフト量を任意に可変する制御手段（６０）とを備えている。

【００１９】また、本発明の請求項４のフェージングシミュレータは、請求項３記載のフェージングシミュレータにおいて、前記減衰回路が、前記雑音発生器から出力された雑音信号に対して減衰処理を行なうことによって、前記遅延回路の出力信号に間接的に減衰を与えることを特徴とする。

【００２０】また、本発明の請求項５のフェージングシミュレータは、請求項１または請求項２または請求項３または請求項４記載のフェージングシミュレータにおいて、前記所定信号をディジタル信号に変換するＡ／Ｄ変換器（３１）を有し、前記遅延回路が、書込アドレスと読出アドレスとを独立に指定できるメモリ（３６）と、前記メモリに対する書込アドレスを所定順に指定して、前記Ａ／Ｄ変換器から出力されたディジタル信号を前記メモリに記憶させる書込手段（３７）と、前記メモリに対する読出アドレスを順次指定して前記メモリに記憶されたディジタル信号を読み出し前記フェージング付加回路へ送出する読出手段（３８）とを備え、前記制御手段は、前記読出手段が前記メモリに指定する読出アドレスを可変制御して、前記メモリに記憶されたディジタル信号が読み出されるまでの遅延時間を任意に可変することを特徴としている。

【００２１】

【発明の実施の形態】以下、図面に基づいて本発明の一実施形態を説明する。図１は、本発明の一実施形態の２パス型のフェージングシミュレータ３０の構成を示している。

【００２２】なお、本発明は１パス型のフェージングシミュレータでも動作する。２パス型の場合には、例えば局間の直接の伝搬ルートと反射波のルートの２ルートの試験が可能であるのに対し、１パス型の場合には、直接の伝搬ルートだけの試験となる。２パス型としては反射波と別の反射波の２伝搬ルートを試験することもできる。また、３パス、４パス、…とパスを増して試験する

こともできる。いずれも原理は同じなので、ここでは２パス型で説明する。

【００２３】図１において、信号発生器１から出力される所定信号は、フェージングシミュレータ３０の入力端子３０ａを介してＡ／Ｄ変換器３１に入力される。

【００２４】Ａ／Ｄ変換器３１は、所定信号をクロック信号Ｃｋに同期する周期でサンプリングしてディジタル信号に変換する。

【００２５】Ａ／Ｄ変換器３１によってディジタル信号に変換された所定信号は分岐されて２つの伝搬路模擬回路３２、３３へ入力される。

【００２６】伝搬路模擬回路３２、３３は同一構成であり、それぞれ遅延回路３５、フェージング付加回路４０、Ｄ／Ａ変換器５０および減衰回路５１によって構成されている。

【００２７】遅延回路３５は、後述する制御部６０とともにこの実施形態の遅延回路を構成するものであり、メモリ３６、書込回路３７および読出回路３８によって構成されている。メモリ３６は書込アドレスと読出アドレスとを独立に指定でき、独立した入出力ポートを有するデュアルポートＲＡＭによって形成されている。

【００２８】書込回路３７は、メモリ３６に対する書込アドレスＡｗをクロック信号Ｃｋに同期して所定順に指定して、Ａ／Ｄ変換器３１から出力されたディジタル信号をメモリ３６に記憶させる。

【００２９】読出回路３８は、メモリに対する読出アドレスＡｒをクロック信号Ｃｋに同期して順次指定してメモリ３６に記憶されたディジタル信号を読み出す。

【００３０】したがって、メモリ３６に書き込まれたディジタル信号は、書込アドレスＡｗと読出アドレスＡｒとの差ΔＡにクロック信号Ｃｋの周期を乗じた時間だけ遅れて読み出される。なお、読出回路３８は、後述する制御部６０からの遅延制御信号に応じて、ΔＡが変化するように読出アドレスＡｒを可変する。

【００３１】フェージング付加回路４０は、後述する制御部６０とともにこの実施形態のフェージング付加回路を構成するものであり、ＤＳＰによって構成された雑音発生器４１から出力されるディジタルの白色雑音信号をオーバサンプリング回路４２に入力する。

【００３２】オーバサンプリング回路４２は、例えば雑音発生器４１から出力された雑音信号系列が〔N_1，N_2，…，N_k，…　〕であれば、これを〔N_1，０，…，０，N_2，０，…，０，…，N_k，０，…，０，…〕のように、各信号間を複数（Ｍ－１）個の０データで補間し、これをディジタルフィルタに通過させることにより、雑音信号の信号成分自体を変化させずにイメージ成分のみを高域にシフトする。このように、信号間をＭ－１個の０データで補間してフィルタリングする方式をＭ倍オーバサンプリングという。

【００３３】さらに詳しく説明すると、雑音発生器４１から出力された雑音信号をオーバサンプリング処理をせずにクロック発生器４４の周波数ｆｓの速度でＤ／Ａ変換した場合、図２に示すように、雑音信号の基本成分Ｒに対して最も周波数が近いイメージ成分I_1が周波数ｆｓを中心に発生する。したがって、このイメージ成分I_1を除去するための低域通過フィルタが必要となる。

【００３４】この低域通過フィルタの高域遮断周波数ｆａは、通常、図２の特性Ｆのように、周波数ｆｓのほぼ１／２に設定されるため、周波数ｆｓの最大値をｆｓｍとすると、周波数がｆｓｍ時の雑音信号の基本成分Ｒの帯域およびフィルタの高域遮断周波数ｆａをｆｓｍ／２に設定した場合、周波数ｆｓを可変させ基本成分Ｒの帯域を狭くすると、イメージ成分I_1が低域通過フィルタを通過してしまう。

【００３５】これに対し、この実施形態のように雑音発生器４１から出力された雑音信号に対してＭ倍オーバサンプリング処理を行うと、図２に示しているように、雑音信号の基本成分Ｒに対して最も周波数が近いイメージ成分I_2が周波数Ｍ・ｆｓを中心に発生する。これにより、後述する低域通過フィルタ４５の高域遮断周波数を固定した状態でも、周波数ｆｓを可変させることにより雑音信号の基本成分Ｒの帯域をほぼｆａ／２からｆｓｍ／２にわたって可変させることができる。

【００３６】このようにしてオーバサンプリング処理された雑音信号は、Ｄ／Ａ変換器４３によってアナログ信号に変換される。Ｄ／Ａ変換器４３は、クロック発生器４４からのクロック信号Ｃｖに同期して雑音信号をアナログ信号に変換して、低域通過フィルタ４５へ出力する。

【００３７】クロック発生器４４は、後述する制御部６０からの雑音制御信号に応じてクロック信号Ｃｖの周波数を可変して、雑音信号の基本成分の帯域を可変させ、雑音信号の波形を変化させる。

【００３８】低域通過フィルタ４５の出力信号は、Ａ／Ｄ変換器４６によってディジタル信号に変換され直交変調器４７に出力される。なお、Ａ／Ｄ変換器４６はクロック信号Ｃｋに同期してディジタル変換を行なう。

【００３９】直交変調器４７は、遅延回路３５のメモリ３６から読み出されたディジタル信号をＡ／Ｄ変換器４６から出力されたディジタルの雑音信号によって変調して、フェージング変動およびドップラシフトを付加する。

【００４０】直交変調器４７から出力された信号は、Ｄ／Ａ変換器５０によってアナログ信号に変換され、減衰回路５１に入力される。

【００４１】減衰回路５１は、制御部６０からの減衰制御信号に応じて直交変調器４７から出力された信号に対する減衰量を変化させる。

【００４２】伝搬路模擬回路３２、３３の各減衰回路５１から出力された信号は、合成回路５２に入力されて合

成され、その合成信号が出力端子３０ｂから評価対象の無線機器２へ出力される。

【００４３】制御部６０は、伝搬路模擬回路３２、３３の遅延回路３５、フェージング付加回路４０および減衰回路５１に対する遅延制御信号、雑音制御信号および減衰制御信号を、予め設定された変動パターンにしたがって連続的に変化させ、例えば、評価対象の無線機器２が移動局の場合には基地局からの電波を移動しながら受信したときの受信信号と同様に変動する合成信号を無線機器２に出力する。

【００４４】このように、実施形態のフェージングシミュレータ３０の遅延処理は、Ａ／Ｄ変換器３１によってディジタル信号に変換された所定信号を、書込アドレスと読出アドレスとを独立に指定できるメモリ３６にアドレス順に記憶し、これをアドレス差のある状態で順次読み出すとともに、書込アドレスに対する読出アドレスの差を可変して信号の遅延時間を可変している。

【００４５】このため、遅延時間を変動する際に直ちに、アドレスの差に対応した正確な遅延時間を与えることができる。

【００４６】また、フェージングシミュレータ３０のフェージング付加処理は、ＤＳＰによる雑音発生器４１から出力された一定のサンプリングレートに対して帯域固定の雑音信号をオーバサンプリング処理してから、Ｄ／Ａ変換してアナログ信号に変換し、この信号から周波数固定の低域通過フィルタ４５によってイメージ成分を除去して直交変調器４７へ入力して、遅延回路３５から出力された信号に対してフェージング変動とドップラシフトを与え、Ｄ／Ａ変換器４３に対するクロック周波数を可変して雑音信号の帯域を可変してフェージング変動量とドップラシフト量を変動させている。

【００４７】このため、精度の高い雑音信号が得られ、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、ＤＳＰのプログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【００４８】

【他の実施の形態】前記実施形態のフェージング付加処理では、雑音信号に対してオーバサンプリング処理を行なうことによって、Ｄ／Ａ変換時に発生する雑音信号のイメージ周波数を高域側にシフトして、周波数固定の低域通過フィルタでそのイメージ周波数を除去していたが、図３に示すフェージング付加回路７０のように、雑音発生器４１から出力された雑音信号をＤ／Ａ変換器４３によってアナログの雑音信号に変換し、この雑音信号に含まれるイメージ成分をスイッチトキャパシタフィルタ（以下、ＳＣＦと記す）７１によって除去するようにしてもよい。

【００４９】なお、ＳＣＦ７１の後段に設けられている低域通過フィルタ（ＬＰＦ）７２は、ＳＣＦ７１の出力からクロック信号Ｃｖ成分を除去するためのものである。

【００５０】ＳＣＦ７１は、クロック信号Ｃｖの周波数に応じた遮断周波数で入力信号に対する帯域制限を行なう帯域可変フィルタ素子であり、低域通過フィルタとして用いた場合、クロック信号Ｃｖの周波数が高くなるとそれに応じて高域遮断周波数が高い方へシフトする。

【００５１】したがって、あるクロック周波数において図４の（ａ）の特性Ｇのように、ＳＣＦ７１の高域遮断周波数ｆｂを雑音信号の基本成分Ｒの帯域より僅かに高い周波数に設定しておけば、図４の（ｂ）のようにクロック信号Ｃｖの周波数を可変したとき、ＳＣＦ７１の高域遮断周波数ｆｂも同一方向に変化し、雑音信号のイメージ成分Ｉを除去してその基本成分Ｒのみを通過させることができ、信号に対する瞬断を発生させることなく、フェージング変動量およびドップラシフト量を変化させることができる。

【００５２】なお、ここでは、ＳＣＦ７１を帯域可変フィルタとして用いているが、Ｄ／Ａ変換器４３のクロック信号の周波数に応じて高域遮断周波数を可変できるものであれば、他の帯域可変フィルタを用いることもできる。

【００５３】また、前記実施形態では、２つの伝搬路模擬回路を有する２パス型のフェージングシミュレータに本発明を適用していたが、本発明は、３パス以上のフェージングシミュレータや、伝搬路模擬回路が１つだけの１パス型のフェージングシミュレータにも同様に適用できる。

【００５４】また、前記実施形態では、遅延処理およびフェージング付加処理が成された信号に対して減衰処理を直接行なうようにしていたが、例えば、図５に示すように、雑音発生器４１から出力された雑音信号をオーバサンプリング回路４２によってオーバサンプリング処理し、オーバサンプリング処理された雑音信号をディジタル型の減衰回路７６に入力して減衰処理を行い、減衰処理した信号をＤ／Ａ変換器４３によってアナログ信号に変換するように構成してもよい。

【００５５】なお、減衰回路７６を雑音発生器４１とオーバサンプリング回路４２の間に設けた場合には、減衰回路がＤ／Ａ変換器４３のクロックに同期して動作してしまうが、図５のように、減衰回路７６をオーバサンプリング回路４２とＤ／Ａ変換器４３の間に設けた場合には、減衰制御とＤ／Ａ変換器４３のクロックの可変制御とを独立に行なえ、減衰処理を遅延なく行なうことができる。

【００５６】なお、図５のようにフェージング付加回路内に減衰回路を設けた場合には、Ｄ／Ａ変換器５０の出力を合成回路５２によって合成して無線機器２へ与える。

【００５７】

【発明の効果】以上説明したように、本発明の請求項１のフェージングシミュレータでは、雑音発生器から出力されたディジタルの雑音信号をオーバサンプリング処理してから、Ｄ／Ａ変換してアナログ信号に変換し、この信号から周波数固定の低域通過フィルタによってイメージ成分を除去し、このイメージ成分を除去した雑音信号によって所定信号を変調するとともに、Ｄ／Ａ変換器に対するクロック周波数を可変して雑音信号の帯域を可変して、所定信号にフェージング変動とドップラシフトを与えている。

【００５７】このため、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、プログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【００５８】また、本発明の請求項３のフェージングシミュレータでは、雑音発生器から出力されたディジタルの雑音信号をＤ／Ａ変換してアナログ信号に変換し、この信号から帯域可変フィルタによってイメージ成分を除去し、このイメージ成分を除去した雑音信号によって所定信号を変調するとともに、Ｄ／Ａ変換器に対するクロック周波数を可変して雑音信号の帯域を可変して、所定信号にフェージング変動とドップラシフトを与えている。

【００５９】このため、精度の高いフェージング変動とドップラシフトを与えることができ、しかも、プログラムを変更することなく雑音信号の帯域を可変でき、信号の瞬断が発生しない。

【００６０】また、本発明の請求項５のフェージングシミュレータでは、上記フェージングシミュレータにおいて、Ａ／Ｄ変換器によってディジタル信号に変換された所定信号を、書込アドレスと読出アドレスとを独立に指定できるメモリにアドレス順に記憶し、これをアドレス差のある状態で順次読み出すとともに、書込アドレスに対する読出アドレスの差を可変して信号の遅延時間を可変している。

【００６１】このため、精度の高いフェージング変動とドップラシフトを与えるとともに、遅延時間を変動する際に直ちにアドレス差に対応した正確な遅延時間を与えることができる。

【図面の簡単な説明】

【図１】本発明の一実施形態の構成を示すブロック図

【図２】一実施形態の動作を説明するための図

【図３】本発明の他の実施形態の構成を示すブロック図

【図４】他の実施形態の動作を説明するための図

【図５】本発明の他の実施形態の構成を示すブロック図

【図６】従来装置の構成を示すブロック図

【符号の説明】

３０　フェージングシミュレータ
３１　Ａ／Ｄ変換器
３２、３３　伝搬路模擬回路
３５　遅延回路
３６　メモリ
３７　書込回路
３８　読出回路
４０　フェージング付加回路
４１　雑音発生器
４２　オーバサンプリング回路
４３　Ｄ／Ａ変換器
４４　クロック発生器
４５　低域通過フィルタ
４６　Ａ／Ｄ変換器
４７　直交変調器
５０　Ｄ／Ａ変換器
５１　減衰回路
５２　合成回路
６０　制御部

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The memory as which it has the A/D converter (31) which changes said Sadanobu Tokoro number into a digital signal, and said delay circuit can specify a write address and the read-out address independently (36), A write-in means to make said memory memorize the digital signal which specified the write address to said memory in predetermined order, and was outputted from said A/D converter (37), A read-out means to read the digital signal which carried out sequential assignment of the read-out address to said memory, and was memorized by said memory, and to send out to said phasing addition circuit (38), The phasing simulator which the aforementioned read-out means carries out adjustable control of the read-out address specified as said memory, and is characterized by having the control means (60) which carries out adjustable [of the time delay until reading appearance of the digital signal memorized by said memory is carried out] to arbitration.
[Claim 2] The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), An exaggerated sampling means to carry out exaggerated sampling processing of said noise signal, and to shift the image component of a noise signal to a high region side (42), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes into an analog signal said noise signal by which exaggerated sampling processing was carried out synchronizing with the clock signal from said clock generation machine (43), The low pass filter which removes said image component from the noise signal changed into the analog signal by said D/A converter (45), The output signal of said delay circuit is modulated with the output signal of said low pass filter. Adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine is carried out. The phasing simulator characterized by having the control means (60) which carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[Claim 3] Said attenuation circuit is a phasing simulator according to claim 2 characterized by giving attenuation indirectly to the output signal of said delay circuit by performing attenuation processing to the output signal of said exaggerated sampling means.
[Claim 4] The delay circuit which performs delay processing to the inputted Sadanobu Tokoro

number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes said noise signal into an analog signal synchronizing with the clock signal from said clock generation machine (43), The band adjustable filter from which the image component contained in the noise signal which the treble cut off frequency changed according to the frequency of the clock signal from said clock generation machine, and was outputted from said D/A converter is removed (71), The output signal of said delay circuit is modulated with the output signal of said band adjustable filter. Adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine is carried out. The phasing simulator characterized by having the control means (60) which carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[Claim 5] The phasing simulator according to claim 4 characterized by giving attenuation indirectly to the output signal of said delay circuit when said attenuation circuit performs attenuation processing to the noise signal outputted from said noise generator.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention performs delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and in the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which performed these processings, in case delay characteristics and a phasing property are changed, it relates to the technique for making it not generate the hits of a signal.
[0002]
[Description of the Prior Art] It is necessary supposing many propagation paths to check actuation of wireless devices, such as a testing-machine machine for examining a terminal, a base station, or them, in the system which communicates by the electric wave.
[0003] Especially, in the case of a mobile station, the propagation property of a propagation path is sharply changed with time amount. The element of fluctuation of this propagation property is attenuation fluctuation by the travelling period difference of a multi-pass, phasing fluctuation, doppler shift fluctuation, a shelter, etc., in order to check actuation of a wireless device, needs to carry out delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and needs to give the signal which performed these processings to a wireless device as a simulation propagation signal.
[0004] Drawing 6 shows the configuration of the phasing simulator 10 of the multi-pass mold generally used for such the object.
[0005] This phasing simulator 10 receives the Sadanobu Tokoro number (signal of the stable analog used for a communication link) outputted from the signal generator 1 through input terminal 10a, branches and inputs this into two propagation path simulation circuits 11 and 12.
[0006] The propagation path simulation circuits 11 and 12 are constituted by the attenuation circuit 21 which gives attenuation to the signal outputted from the delay circuit 13 delayed in a predetermined signal, the phasing addition circuit 17 which gives phasing fluctuation and a doppler shift to the signal outputted from the delay circuit 13, and the phasing addition circuit 17.
[0007] The delay circuit 13 is constituted by A/D converter 14 which changes an input signal into a digital signal, the shift register 15 which undergoes the output of A/D converter 14 and is made to generate fixed delay, and D/A converter 16 which changes the output from a shift register 15 into an analog signal, and changes the time delay over a Sadanobu Tokoro number by carrying out adjustable [of the number of stages of a shift register 15] with the control signal from the control section which is not illustrated.
[0008] The phasing addition circuit 17 is constituted by the noise generator 18, D/A converter 19, and the quadrature modulation machine 20, and with D/A converter 19, the digital white-noise signal outputted from a noise generator 18 is changed into the noise signal of an analog, and it outputs it to the quadrature modulation machine 20.
[0009] With the noise signal outputted from D/A converter 19, the quadrature modulation machine 20 modulates the amplitude and phase of a predetermined signal, and gives phasing

fluctuation and a doppler shift.
[0010] This phasing addition circuit 17 changes the amount of phasing fluctuation and the amount of doppler shifts to a predetermined signal by changing the program of a noise generator 18 with the control signal from a control section.
[0011] Moreover, an attenuation circuit 21 changes the magnitude of attenuation to the signal outputted from the phasing addition circuit 17 by the control signal from a control section.
[0012] Thus, the output of two constituted propagation path simulation circuits 11 and 12 is equivalent to the electric wave which was discharged from the same transmitter and passed through two different propagation paths, and can check actuation of the wireless device 2 by the actual busy condition by inputting into the wireless device 2 for assessment the composite signal which compounded both the output by the synthetic circuit 22 from output terminal 10b.
[0013]
[Problem(s) to be Solved by the Invention] However, by the above mentioned conventional phasing simulator, whenever it changes the amount of phasing fluctuation etc., the program of a noise generator will have to be changed, and the hits of a signal will occur between program modification.
[0014] Moreover, by the approach of changing the number of stages of a shift register like the above mentioned delay circuit, and carrying out adjustable [of the time delay], even if it changes the number of stages of a shift register for time delay modification, the delay signal meant promptly may not be outputted and trouble is in the check of a wireless device of operation.
[0015] This invention aims at offering the phasing simulator which solved these problems.
[0016]
[Means for Solving the Problem] In order to attain said object, the phasing simulator of claim 1 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The memory as which it has the A/D converter (31) which changes said Sadanobu Tokoro number into a digital signal, and said delay circuit can specify a write address and the read-out address independently (36), A write-in means to make said memory memorize the digital signal which specified the write address to said memory in predetermined order, and was outputted from said A/D converter (37), A read-out means to read the digital signal which carried out sequential assignment of the read-out address to said memory, and was memorized by said memory, and to send out to said phasing addition circuit (38), The aforementioned read-out means carried out adjustable control of the read-out address specified as said memory, and it has the control means (60) which carries out adjustable [of the time delay until reading appearance of the digital signal memorized by said memory is carried out] to arbitration.
[0017] Moreover, the phasing simulator of claim 2 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), An exaggerated sampling means to carry out exaggerated sampling processing of said noise signal, and to shift the image component of a noise signal to a high region side (42), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes into an analog signal said noise signal by which exaggerated sampling processing was carried out synchronizing with the clock signal from said clock generation machine (43), The low pass filter which removes said image component from the noise signal changed into the analog signal by said D/A converter (45), The output signal of

said delay circuit is modulated with the output signal of said low pass filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[0018] Moreover, the phasing simulator of claim 3 of this invention is characterized by said attenuation circuit giving attenuation indirectly to the output signal of said delay circuit by performing attenuation processing to the output signal of said exaggerated sampling means in a phasing simulator according to claim 2.
[0019] Moreover, the phasing simulator of claim 4 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes said noise signal into an analog signal synchronizing with the clock signal from said clock generation machine (43), The band adjustable filter from which the image component contained in the noise signal which the treble cut off frequency changed according to the frequency of the clock signal from said clock generation machine, and was outputted from said D/A converter is removed (71), The output signal of said delay circuit is modulated with the output signal of said band adjustable filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[0020] Moreover, in a phasing simulator according to claim 4, the phasing simulator of claim 5 of this invention is characterized by giving attenuation indirectly to the output signal of said delay circuit, when said attenuation circuit performs attenuation processing to the noise signal outputted from said noise generator.
[0021]
[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained based on a drawing. Drawing 1 shows the configuration of the phasing simulator 30 of the two pass mold of 1 operation gestalt of this invention.
[0022] In addition, this invention operates also by the phasing simulator of an one-pass mold. In the case of a two pass mold, in the case of an one-pass mold, it becomes with the trial of only the direct propagation root to the trial of the 2 roots of the direct propagation root for example, between stations and the root of a reflected wave being possible. 2 propagation root of a reflected wave other than a reflected wave as a two pass mold can also be examined. Moreover, pass is increased with three pass, four pass, and --, and it can also examine. Since all of a principle are the same, a two pass mold explains here.
[0023] In drawing 1 , the Sadanobu Tokoro number outputted from a signal generator 1 is inputted into A/D converter 31 through input terminal 30a of the phasing simulator 30.
[0024] A/D converter 31 samples a predetermined signal with the period which synchronizes with a clock signal Ck, and changes it into a digital signal.
[0025] The Sadanobu Tokoro number changed into the digital signal branches, and is inputted into two propagation path simulation circuits 32 and 33 by A/D converter 31.
[0026] The propagation path simulation circuits 32 and 33 are the same configurations, and are constituted by the delay circuit 35, the phasing addition circuit 40, D/A converter 50, and the attenuation circuit 51, respectively.
[0027] A delay circuit 35 constitutes the delay circuit of this operation gestalt with the control section 60 mentioned later, and is constituted by memory 36, the write-in circuit 37, and the read-out circuit 38. Memory 36 can specify a write address and the read-out address

independently, and is formed by the dual port RAM which has independent input/output port.
[0028] The write-in circuit 37 specifies the write address Aw to memory 36 in predetermined order synchronizing with a clock signal Ck, and makes memory 36 memorize the digital signal outputted from A/D converter 31.
[0029] The read-out circuit 38 reads the digital signal which carried out sequential assignment of the read-out address Ar to memory synchronizing with the clock signal Ck, and was memorized by memory 36.
[0030] Therefore, only the time amount which multiplied by the period of a clock signal Ck is behind [difference deltaA of a write address Aw and the read-out address Ar] in the digital signal written in memory 36, and reading appearance is carried out to it. In addition, according to the delay control signal from a control section 60 mentioned later, the read-out circuit 38 carries out adjustable [of the read-out address Ar] so that deltaA may change.
[0031] The phasing addition circuit 40 inputs into the exaggerated sampling circuit 42 the digital white-noise signal outputted from the noise generator 41 which constitutes the phasing addition circuit of this operation gestalt with the control section 60 mentioned later, and was constituted by DSP.
[0032] If the noise signal sequences outputted from the noise generator 41 are [N1, N2, --, Nk, --], the exaggerated sampling circuit 42 This like [N1, 0, --, 0N2, 0, --, 0, --, Nk, 0, --, 0, --] Only an image component is shifted to a high region by interpolating between each signal by zero data of two or more (M-1) individuals, and making a digital filter pass this, without changing the signal component of a noise signal itself. Thus, the method which interpolates and filters between signals by M-1 data [zero] is called exaggerated sampling M times.
[0033] It is [as opposed to / when are explained in more detail and D/A conversion of the noise signal outputted from the noise generator 41 is carried out at the rate of the frequency fs of the clock generation machine 44, without carrying out exaggerated sampling processing, as it is shown in drawing 2 / the fundamental component R of a noise signal] the image component I1 with the nearest frequency. It generates focusing on a frequency fs. Therefore, this image component I1 The low pass filter for removing is needed.
[0034] Like the property F of drawing 2 , the treble cut off frequency fa of this low pass filter is usually the image component I1, when maximum of a frequency fs was set to fsm, the band of the fundamental component R of a noise signal it is whose frequency at the fsm time, and the treble cut off frequency fa of a filter are set as fsm/2, adjustable [of the frequency fs] is carried out and the band of a fundamental component R is narrowed, since [of a frequency fs] about 1/was set as 2. A low pass filter will be passed.
[0035] On the other hand, when exaggerated sampling processing is performed M times to the noise signal outputted from the noise generator 41 like this operation gestalt, it is [as opposed to / as shown in drawing 2 / the fundamental component R of a noise signal] the image component I2 with the nearest frequency. It generates focusing on frequency M-fs. Also after this has fixed the treble cut off frequency of the low pass filter 45 mentioned later, ranging from fa/2 to fsm/2, it can carry out adjustable [of the band of the fundamental component R of a noise signal] mostly by carrying out adjustable [of the frequency fs].
[0036] Thus, the noise signal by which exaggerated sampling processing was carried out is changed into an analog signal by D/A converter 43. D/A converter 43 changes a noise signal into an analog signal synchronizing with clock signal Cv from the clock generation machine 44, and outputs it to a low pass filter 45.
[0037] The clock generation machine 44 carries out adjustable [of the frequency of clock signal Cv] according to the noise control signal from a control section 60 mentioned later, carries out adjustable [of the band of the fundamental component of a noise signal], and changes the wave of a noise signal.
[0038] The output signal of a low pass filter 45 is changed into a digital signal by A/D converter 46, and is outputted to the quadrature modulation machine 47 by it. In addition, A/D converter 46 performs digital conversion synchronizing with a clock signal Ck.
[0039] The quadrature modulation machine 47 modulates the digital signal by which reading appearance was carried out from the memory 36 of a delay circuit 35 with the digital noise signal

outputted from A/D converter 46, and adds phasing fluctuation and a doppler shift.
[0040] The signal outputted from the quadrature modulation machine 47 is changed into an analog signal by D/A converter 50, and is inputted into an attenuation circuit 51.
[0041] An attenuation circuit 51 changes the magnitude of attenuation to the signal outputted from the quadrature modulation machine 47 according to the attenuation control signal from a control section 60.
[0042] The signal outputted from each attenuation circuit 51 of the propagation path simulation circuits 32 and 33 is inputted and compounded by the synthetic circuit 52, and the composite signal is outputted to the wireless device 2 for assessment from output terminal 30b.
[0043] A control section 60 outputs the input signal when receiving moving [according to the fluctuation pattern set up beforehand, changed continuously the delay control signal, noise control signal, and attenuation control signal over the delay circuit 35, the phasing addition circuit 40, and attenuation circuit 51 of the propagation path simulation circuits 32 and 33, for example,] the electric wave from a base station, when the wireless device 2 for assessment is a mobile station, and the composite signal changed similarly to the wireless device 2.
[0044] Thus, delay processing of the phasing simulator 30 of an operation gestalt memorizes the Sadanobu Tokoro number changed into the digital signal by A/D converter 31 in order of the address in the memory 36 which can specify a write address and the read-out address independently, carries out adjustable [of the difference of the read-out address to a write address], and is carrying out adjustable [of the time delay of a signal] while it reads this one by one in the condition that there is an address difference.
[0045] For this reason, in case a time delay is changed, the exact time delay corresponding to the difference of the address can be given promptly.
[0046] Moreover, phasing attached processing of the phasing simulator 30 After carrying out exaggerated sampling processing of the noise signal of band immobilization to the fixed sampling rate outputted from the noise generator 41 by DSP Carry out D/A conversion, change into an analog signal, the low pass filter 45 of frequency immobilization removes an image component from this signal, and it inputs into the quadrature modulation machine 47. Phasing fluctuation and a doppler shift are given to the signal outputted from the delay circuit 35, adjustable [of the clock frequency to D/A converter 43] is carried out, adjustable [of the band of a noise signal] is carried out, and the amount of phasing fluctuation and the amount of doppler shifts are fluctuated.
[0047] For this reason, a noise signal with a high precision is acquired, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing the program of DSP, and the hits of a signal do not occur.
[0048]
[The gestalt of other operations] Although the image frequency of the noise signal generated by performing exaggerated sampling processing to a noise signal at the time of D/A conversion was shifted to the high region side and the low pass filter of frequency immobilization had removed the image frequency in phasing attached processing of said operation gestalt The noise signal outputted from the noise generator 41 is changed into the noise signal of an analog with D/A converter 43 like the phasing addition circuit 70 shown in drawing 3 . You may make it a switched capacitor filter (for it to be hereafter described as SCF) 71 remove the image component contained in this noise signal.
[0049] In addition, the low pass filter (LPF) 72 prepared in the latter part of SCF71 is for removing a clock signal Cv component from the output of SCF71.
[0050] SCF71 is a band adjustable filter element which performs the band limit to an input signal with the cut-off frequency according to the frequency of clock signal Cv, and when it uses as a low pass filter, if the frequency of clock signal Cv becomes high, according to it, a treble cut off frequency will shift it to the higher one.
[0051] In a certain clock frequency therefore, like the property G of (a) of drawing 4 If the treble cut off frequency fb of SCF71 is set as the frequency slightly higher than the band of the fundamental component R of a noise signal As shown in (b) of drawing 4 , when it carries out

adjustable [of the frequency of clock signal Cv], the treble cut off frequency fb of SCF71 also changes in the same direction. The amount of phasing fluctuation and the amount of doppler shifts can be changed without being able to remove the image component I of a noise signal, being able to pass the fundamental component R, and generating the hits to a signal.
[0052] In addition, although SCF71 is used as a band adjustable filter, if it can carry out adjustable [of the treble cut off frequency] according to the frequency of the clock signal of D/A converter 43, other band adjustable filters can also be used here.
[0053] Moreover, although this invention was applied to the phasing simulator of the two pass mold which has two propagation path simulation circuits with said operation gestalt, the phasing simulator and propagation path simulation circuit of 3 or more ****s can apply this invention also like the phasing simulator of only one one-pass mold.
[0054] Moreover, although it is made to perform attenuation processing directly with said operation gestalt to the signal which delay processing and phasing attached processing constituted For example, as shown in drawing 5 , exaggerated sampling processing of the noise signal outputted from the noise generator 41 is carried out by the exaggerated sampling circuit 42. You may constitute so that the noise signal by which exaggerated sampling processing was carried out may be inputted into the attenuation circuit 76 of a digital mold, attenuation processing may be performed and the signal which carried out attenuation processing may be changed into an analog signal with D/A converter 43.
[0055] In addition, when an attenuation circuit 76 is formed between a noise generator 41 and the exaggerated sampling circuit 42, an attenuation circuit will operate synchronizing with the clock of D/A converter 43, but like drawing 5 , when an attenuation circuit 76 is formed between the exaggerated sampling circuit 42 and D/A converter 43, attenuation control and adjustable control of the clock of D/A converter 43 can be performed independently, and attenuation processing can be performed without delay.
[0056] In addition, when an attenuation circuit is prepared in a phasing addition circuit like drawing 5 , the output of D/A converter 50 is compounded by the synthetic circuit 52, and it gives to the wireless device 2.
[0057]
[Effect of the Invention] As explained above, by the phasing simulator of claim 1 of this invention, the Sadanobu Tokoro number changed into the digital signal by the A/D converter is memorized in order of the address in the memory which can specify a write address and the read-out address independently, and while reading this one by one in the condition that there is an address difference, adjustable [of the difference of the read-out address to a write address] is carried out, and it is carrying out adjustable [of the time delay of a signal].
[0058] For this reason, in case a time delay is changed, the exact time delay corresponding to the difference of the address can be given promptly.
[0059] moreover, by the phasing simulator of claim 2 of this invention After carrying out exaggerated sampling processing of the digital noise signal outputted from the noise generator While modulating a Sadanobu Tokoro number with the noise signal which carried out D/A conversion, changed into the analog signal, removed the image component from this signal with the low pass filter of frequency immobilization, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are given to the predetermined signal.
[0060] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.
[0061] moreover, by the phasing simulator of claim 4 of this invention Carry out D/A conversion of the digital noise signal outputted from the noise generator, and it changes into an analog signal. While modulating a Sadanobu Tokoro number with the noise signal which removed the image component from this signal with the band adjustable filter, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are

given to the predetermined signal.
[0062] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention performs delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and in the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which performed these processings, in case delay characteristics and a phasing property are changed, it relates to the technique for making it not generate the hits of a signal.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] It is necessary supposing many propagation paths to check actuation of wireless devices, such as a testing-machine machine for examining a terminal, a base station, or them, in the system which communicates by the electric wave.
[0003] Especially, in the case of a mobile station, the propagation property of a propagation path is sharply changed with time amount. The element of fluctuation of this propagation property is attenuation fluctuation by the travelling period difference of a multi-pass, phasing fluctuation, doppler shift fluctuation, a shelter, etc., in order to check actuation of a wireless device, needs to carry out delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and needs to give the signal which performed these processings to a wireless device as a simulation propagation signal.
[0004] Drawing 6 shows the configuration of the phasing simulator 10 of the multi-pass mold generally used for such the object.
[0005] This phasing simulator 10 receives the Sadanobu Tokoro number (signal of the stable analog used for a communication link) outputted from the signal generator 1 through input terminal 10a, branches and inputs this into two propagation path simulation circuits 11 and 12.
[0006] The propagation path simulation circuits 11 and 12 are constituted by the attenuation circuit 21 which gives attenuation to the signal outputted from the delay circuit 13 delayed in a predetermined signal, the phasing addition circuit 17 which gives phasing fluctuation and a doppler shift to the signal outputted from the delay circuit 13, and the phasing addition circuit 17.
[0007] The delay circuit 13 is constituted by A/D converter 14 which changes an input signal into a digital signal, the shift register 15 which undergoes the output of A/D converter 14 and is made to generate fixed delay, and D/A converter 16 which changes the output from a shift register 15 into an analog signal, and changes the time delay over a Sadanobu Tokoro number by carrying out adjustable [of the number of stages of a shift register 15] with the control signal from the control section which is not illustrated.
[0008] The phasing addition circuit 17 is constituted by the noise generator 18, D/A converter 19, and the quadrature modulation machine 20, and with D/A converter 19, the digital white-noise signal outputted from a noise generator 18 is changed into the noise signal of an analog, and it outputs it to the quadrature modulation machine 20.
[0009] With the noise signal outputted from D/A converter 19, the quadrature modulation machine 20 modulates the amplitude and phase of a predetermined signal, and gives phasing fluctuation and a doppler shift.
[0010] This phasing addition circuit 17 changes the amount of phasing fluctuation and the amount of doppler shifts to a predetermined signal by changing the program of a noise generator 18 with the control signal from a control section.
[0011] Moreover, an attenuation circuit 21 changes the magnitude of attenuation to the signal outputted from the phasing addition circuit 17 by the control signal from a control section.
[0012] Thus, the output of two constituted propagation path simulation circuits 11 and 12 is equivalent to the electric wave which was discharged from the same transmitter and passed through two different propagation paths, and can check actuation of the wireless device 2 by the

actual busy condition by inputting into the wireless device 2 for assessment the composite signal which compounded both the output by the synthetic circuit 22 from output terminal 10b.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, by the phasing simulator of claim 1 of this invention, the Sadanobu Tokoro number changed into the digital signal by the A/D converter is memorized in order of the address in the memory which can specify a write address and the read-out address independently, and while reading this one by one in the condition that there is an address difference, adjustable [of the difference of the read-out address to a write address] is carried out, and it is carrying out adjustable [of the time delay of a signal].
[0058] For this reason, in case a time delay is changed, the exact time delay corresponding to the difference of the address can be given promptly.
[0059] moreover, by the phasing simulator of claim 2 of this invention After carrying out exaggerated sampling processing of the digital noise signal outputted from the noise generator While modulating a Sadanobu Tokoro number with the noise signal which carried out D/A conversion, changed into the analog signal, removed the image component from this signal with the low pass filter of frequency immobilization, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are given to the predetermined signal.
[0060] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.
[0061] moreover, by the phasing simulator of claim 4 of this invention Carry out D/A conversion of the digital noise signal outputted from the noise generator, and it changes into an analog signal. While modulating a Sadanobu Tokoro number with the noise signal which removed the image component from this signal with the band adjustable filter, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are given to the predetermined signal.
[0062] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the above mentioned conventional phasing simulator, whenever it changes the amount of phasing fluctuation etc., the program of a noise generator will have to be changed, and the hits of a signal will occur between program modification.
[0014] Moreover, by the approach of changing the number of stages of a shift register like the above mentioned delay circuit, and carrying out adjustable [of the time delay], even if it changes the number of stages of a shift register for time delay modification, the delay signal meant promptly may not be outputted and trouble is in the check of a wireless device of operation.
[0015] This invention aims at offering the phasing simulator which solved these problems.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain said object, the phasing simulator of claim 1 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The memory as which it has the A/D converter (31) which changes said Sadanobu Tokoro number into a digital signal, and said delay circuit can specify a write address and the read-out address independently (36), A write-in means to make said memory memorize the digital signal which specified the write address to said memory in predetermined order, and was outputted from said A/D converter (37), A read-out means to read the digital signal which carried out sequential assignment of the read-out address to said memory, and was memorized by said memory, and to send out to said phasing addition circuit (38), The aforementioned read-out means carried out adjustable control of the read-out address specified as said memory, and it has the control means (60) which carries out adjustable [of the time delay until reading appearance of the digital signal memorized by said memory is carried out] to arbitration.
[0017] Moreover, the phasing simulator of claim 2 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), An exaggerated sampling means to carry out exaggerated sampling processing of said noise signal, and to shift the image component of a noise signal to a high region side (42), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes into an analog signal said noise signal by which exaggerated sampling processing was carried out synchronizing with the clock signal from said clock generation machine (43), The low pass filter which removes said image component from the noise signal changed into the analog signal by said D/A converter (45), The output signal of said delay circuit is modulated with the output signal of said low pass filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[0018] Moreover, the phasing simulator of claim 3 of this invention is characterized by said attenuation circuit giving attenuation indirectly to the output signal of said delay circuit by performing attenuation processing to the output signal of said exaggerated sampling means in a phasing simulator according to claim 2.
[0019] Moreover, the phasing simulator of claim 4 of this invention The delay circuit which

performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes said noise signal into an analog signal synchronizing with the clock signal from said clock generation machine (43), The band adjustable filter from which the image component contained in the noise signal which the treble cut off frequency changed according to the frequency of the clock signal from said clock generation machine, and was outputted from said D/A converter is removed (71), The output signal of said delay circuit is modulated with the output signal of said band adjustable filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.

[0020] Moreover, in a phasing simulator according to claim 4, the phasing simulator of claim 5 of this invention is characterized by giving attenuation indirectly to the output signal of said delay circuit, when said attenuation circuit performs attenuation processing to the noise signal outputted from said noise generator.

[0021]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained based on a drawing. Drawing 1 shows the configuration of the phasing simulator 30 of the two pass mold of 1 operation gestalt of this invention.

[0022] In addition, this invention operates also by the phasing simulator of an one-pass mold. In the case of a two pass mold, in the case of an one-pass mold, it becomes with the trial of only the direct propagation root to the trial of the 2 roots of the direct propagation root for example, between stations and the root of a reflected wave being possible. 2 propagation root of a reflected wave other than a reflected wave as a two pass mold can also be examined. Moreover, pass is increased with three pass, four pass, and --, and it can also examine. Since all of a principle are the same, a two pass mold explains here.

[0023] In drawing 1 , the Sadanobu Tokoro number outputted from a signal generator 1 is inputted into A/D converter 31 through input terminal 30a of the phasing simulator 30.

[0024] A/D converter 31 samples a predetermined signal with the period which synchronizes with a clock signal Ck, and changes it into a digital signal.

[0025] The Sadanobu Tokoro number changed into the digital signal branches, and is inputted into two propagation path simulation circuits 32 and 33 by A/D converter 31.

[0026] The propagation path simulation circuits 32 and 33 are the same configurations, and are constituted by the delay circuit 35, the phasing addition circuit 40, D/A converter 50, and the attenuation circuit 51, respectively.

[0027] A delay circuit 35 constitutes the delay circuit of this operation gestalt with the control section 60 mentioned later, and is constituted by memory 36, the write-in circuit 37, and the read-out circuit 38. Memory 36 can specify a write address and the read-out address independently, and is formed by the dual port RAM which has independent input/output port.

[0028] The write-in circuit 37 specifies the write address Aw to memory 36 in predetermined order synchronizing with a clock signal Ck, and makes memory 36 memorize the digital signal outputted from A/D converter 31.

[0029] The read-out circuit 38 reads the digital signal which carried out sequential assignment of the read-out address Ar to memory synchronizing with the clock signal Ck, and was memorized by memory 36.

[0030] Therefore, only the time amount which multiplied by the period of a clock signal Ck is behind [difference deltaA of a write address Aw and the read-out address Ar] in the digital signal written in memory 36, and reading appearance is carried out to it. In addition, according to

the delay control signal from a control section 60 mentioned later, the read-out circuit 38 carries out adjustable [of the read-out address Ar] so that deltaA may change.
[0031] The phasing addition circuit 40 inputs into the exaggerated sampling circuit 42 the digital white-noise signal outputted from the noise generator 41 which constitutes the phasing addition circuit of this operation gestalt with the control section 60 mentioned later, and was constituted by DSP.
[0032] If the noise signal sequences outputted from the noise generator 41 are [N1, N2, --, Nk, --], the exaggerated sampling circuit 42 This like [N1, 0, --, 0N2, 0, --, 0, --, Nk, 0, --, 0, --] Only an image component is shifted to a high region by interpolating between each signal by zero data of two or more (M-1) individuals, and making a digital filter pass this, without changing the signal component of a noise signal itself. Thus, the method which interpolates and filters between signals by M-1 data [zero] is called exaggerated sampling M times.
[0033] It is [as opposed to / when are explained in more detail and D/A conversion of the noise signal outputted from the noise generator 41 is carried out at the rate of the frequency fs of the clock generation machine 44, without carrying out exaggerated sampling processing, as it is shown in drawing 2 / the fundamental component R of a noise signal] the image component I1 with the nearest frequency. It generates focusing on a frequency fs. Therefore, this image component I1 The low pass filter for removing is needed.
[0034] Like the property F of drawing 2 , the treble cut off frequency fa of this low pass filter is usually the image component I1, when maximum of a frequency fs was set to fsm, the band of the fundamental component R of a noise signal it is whose frequency at the fsm time, and the treble cut off frequency fa of a filter are set as fsm/2, adjustable [of the frequency fs] is carried out and the band of a fundamental component R is narrowed, since [of a frequency fs] about 1/was set as 2. A low pass filter will be passed.
[0035] On the other hand, when exaggerated sampling processing is performed M times to the noise signal outputted from the noise generator 41 like this operation gestalt, it is [as opposed to / as shown in drawing 2 / the fundamental component R of a noise signal] the image component I2 with the nearest frequency. It generates focusing on frequency M-fs. Also after this has fixed the treble cut off frequency of the low pass filter 45 mentioned later, ranging from fa/2 to fsm/2, it can carry out adjustable [of the band of the fundamental component R of a noise signal] mostly by carrying out adjustable [of the frequency fs].
[0036] Thus, the noise signal by which exaggerated sampling processing was carried out is changed into an analog signal by D/A converter 43. D/A converter 43 changes a noise signal into an analog signal synchronizing with clock signal Cv from the clock generation machine 44, and outputs it to a low pass filter 45.
[0037] The clock generation machine 44 carries out adjustable [of the frequency of clock signal Cv] according to the noise control signal from a control section 60 mentioned later, carries out adjustable [of the band of the fundamental component of a noise signal], and changes the wave of a noise signal.
[0038] The output signal of a low pass filter 45 is changed into a digital signal by A/D converter 46, and is outputted to the quadrature modulation machine 47 by it. In addition, A/D converter 46 performs digital conversion synchronizing with a clock signal Ck.
[0039] The quadrature modulation machine 47 modulates the digital signal by which reading appearance was carried out from the memory 36 of a delay circuit 35 with the digital noise signal outputted from A/D converter 46, and adds phasing fluctuation and a doppler shift.
[0040] The signal outputted from the quadrature modulation machine 47 is changed into an analog signal by D/A converter 50, and is inputted into an attenuation circuit 51.
[0041] An attenuation circuit 51 changes the magnitude of attenuation to the signal outputted from the quadrature modulation machine 47 according to the attenuation control signal from a control section 60.
[0042] The signal outputted from each attenuation circuit 51 of the propagation path simulation circuits 32 and 33 is inputted and compounded by the synthetic circuit 52, and the composite signal is outputted to the wireless device 2 for assessment from output terminal 30b.
[0043] A control section 60 outputs the input signal when receiving moving [according to the

fluctuation pattern set up beforehand, changed continuously the delay control signal, noise control signal, and attenuation control signal over the delay circuit 35, the phasing addition circuit 40, and attenuation circuit 51 of the propagation path simulation circuits 32 and 33, for example,] the electric wave from a base station, when the wireless device 2 for assessment is a mobile station, and the composite signal changed similarly to the wireless device 2.
[0044] Thus, delay processing of the phasing simulator 30 of an operation gestalt memorizes the Sadanobu Tokoro number changed into the digital signal by A/D converter 31 in order of the address in the memory 36 which can specify a write address and the read-out address independently, carries out adjustable [of the difference of the read-out address to a write address], and is carrying out adjustable [of the time delay of a signal] while it reads this one by one in the condition that there is an address difference.
[0045] For this reason, in case a time delay is changed, the exact time delay corresponding to the difference of the address can be given promptly.
[0046] Moreover, phasing attached processing of the phasing simulator 30 After carrying out exaggerated sampling processing of the noise signal of band immobilization to the fixed sampling rate outputted from the noise generator 41 by DSP Carry out D/A conversion, change into an analog signal, the low pass filter 45 of frequency immobilization removes an image component from this signal, and it inputs into the quadrature modulation machine 47. Phasing fluctuation and a doppler shift are given to the signal outputted from the delay circuit 35, adjustable [of the clock frequency to D/A converter 43] is carried out, adjustable [of the band of a noise signal] is carried out, and the amount of phasing fluctuation and the amount of doppler shifts are fluctuated.
[0047] For this reason, a noise signal with a high precision is acquired, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing the program of DSP, and the hits of a signal do not occur.
[0048]
[The gestalt of other operations] Although the image frequency of the noise signal generated by performing exaggerated sampling processing to a noise signal at the time of D/A conversion was shifted to the high region side and the low pass filter of frequency immobilization had removed the image frequency in phasing attached processing of said operation gestalt The noise signal outputted from the noise generator 41 is changed into the noise signal of an analog with D/A converter 43 like the phasing addition circuit 70 shown in drawing 3 . You may make it a switched capacitor filter (for it to be hereafter described as SCF) 71 remove the image component contained in this noise signal.
[0049] In addition, the low pass filter (LPF) 72 prepared in the latter part of SCF71 is for removing a clock signal Cv component from the output of SCF71.
[0050] SCF71 is a band adjustable filter element which performs the band limit to an input signal with the cut-off frequency according to the frequency of clock signal Cv, and when it uses as a low pass filter, if the frequency of clock signal Cv becomes high, according to it, a treble cut off frequency will shift it to the higher one.
[0051] In a certain clock frequency therefore, like the property G of (a) of drawing 4 If the treble cut off frequency fb of SCF71 is set as the frequency slightly higher than the band of the fundamental component R of a noise signal As shown in (b) of drawing 4 , when it carries out adjustable [of the frequency of clock signal Cv], the treble cut off frequency fb of SCF71 also changes in the same direction. The amount of phasing fluctuation and the amount of doppler shifts can be changed without being able to remove the image component I of a noise signal, being able to pass the fundamental component R, and generating the hits to a signal.
[0052] In addition, although SCF71 is used as a band adjustable filter, if it can carry out adjustable [of the treble cut off frequency] according to the frequency of the clock signal of D/A converter 43, other band adjustable filters can also be used here.
[0053] Moreover, although this invention was applied to the phasing simulator of the two pass mold which has two propagation path simulation circuits with said operation gestalt, the phasing simulator and propagation path simulation circuit of 3 or more ****s can apply this invention

also like the phasing simulator of only one one-pass mold.

[0054] Moreover, although it is made to perform attenuation processing directly with said operation gestalt to the signal which delay processing and phasing attached processing constituted For example, as shown in drawing 5 , exaggerated sampling processing of the noise signal outputted from the noise generator 41 is carried out by the exaggerated sampling circuit 42. You may constitute so that the noise signal by which exaggerated sampling processing was carried out may be inputted into the attenuation circuit 76 of a digital mold, attenuation processing may be performed and the signal which carried out attenuation processing may be changed into an analog signal with D/A converter 43.

[0055] In addition, when an attenuation circuit 76 is formed between a noise generator 41 and the exaggerated sampling circuit 42, an attenuation circuit will operate synchronizing with the clock of D/A converter 43, but like drawing 5 , when an attenuation circuit 76 is formed between the exaggerated sampling circuit 42 and D/A converter 43, attenuation control and adjustable control of the clock of D/A converter 43 can be performed independently, and attenuation processing can be performed without delay.

[0056] In addition, when an attenuation circuit is prepared in a phasing addition circuit like drawing 5 , the output of D/A converter 50 is compounded by the synthetic circuit 52, and it gives to the wireless device 2.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the configuration of 1 operation gestalt of this invention
[Drawing 2] Drawing for explaining actuation of 1 operation gestalt
[Drawing 3] The block diagram showing the configuration of other operation gestalten of this invention
[Drawing 4] Drawing for explaining actuation of other operation gestalten
[Drawing 5] The block diagram showing the configuration of other operation gestalten of this invention
[Drawing 6] The block diagram showing the configuration of equipment conventionally
[Description of Notations]
30 Phasing Simulator
31 A/D Converter
32 33 Propagation path simulation circuit
35 Delay Circuit
36 Memory
37 Write-in Circuit
38 Read-out Circuit
40 Phasing Addition Circuit
41 Noise Generator
42 Exaggerated Sampling Circuit
43 D/A Converter
44 Clock Generation Machine
45 Low Pass Filter
46 A/D Converter
47 Quadrature Modulation Machine
50 D/A Converter
51 Attenuation Circuit
52 Synthetic Circuit
60 Control Section

[Translation done.]

* NOTICES *

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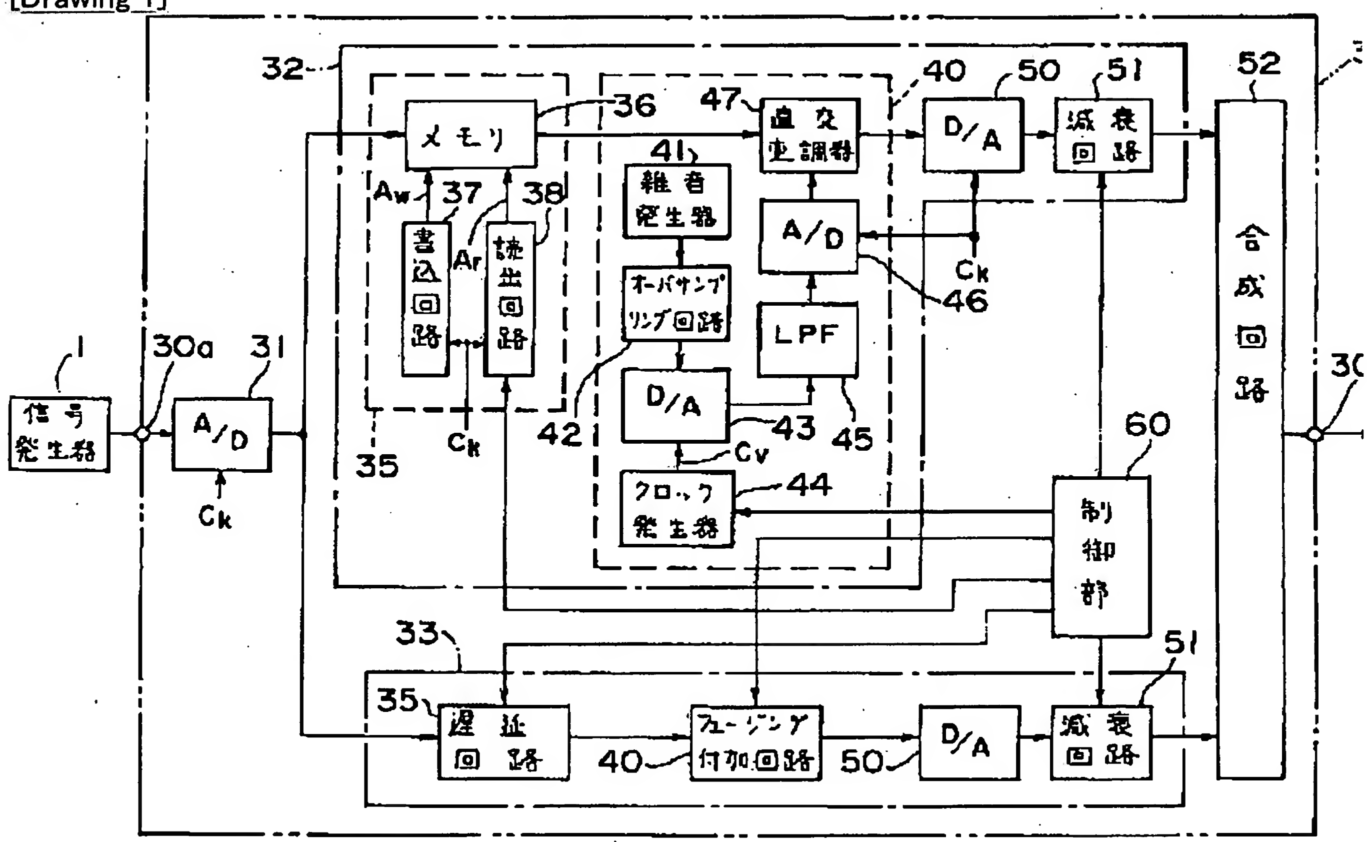
damages caused by the use of this translation.

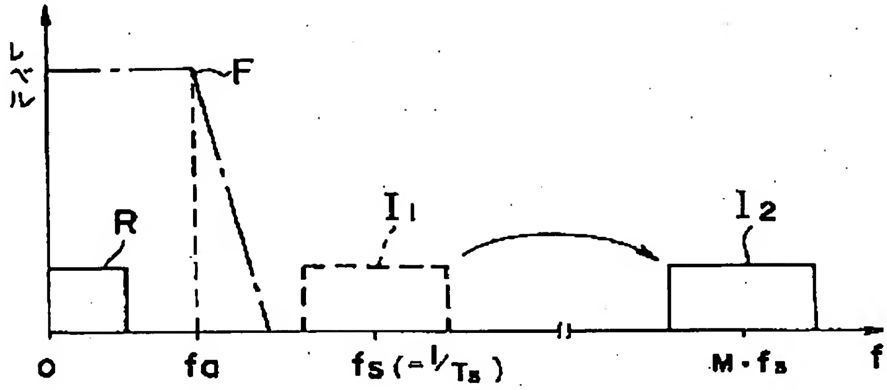
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

WRITTEN AMENDMENT

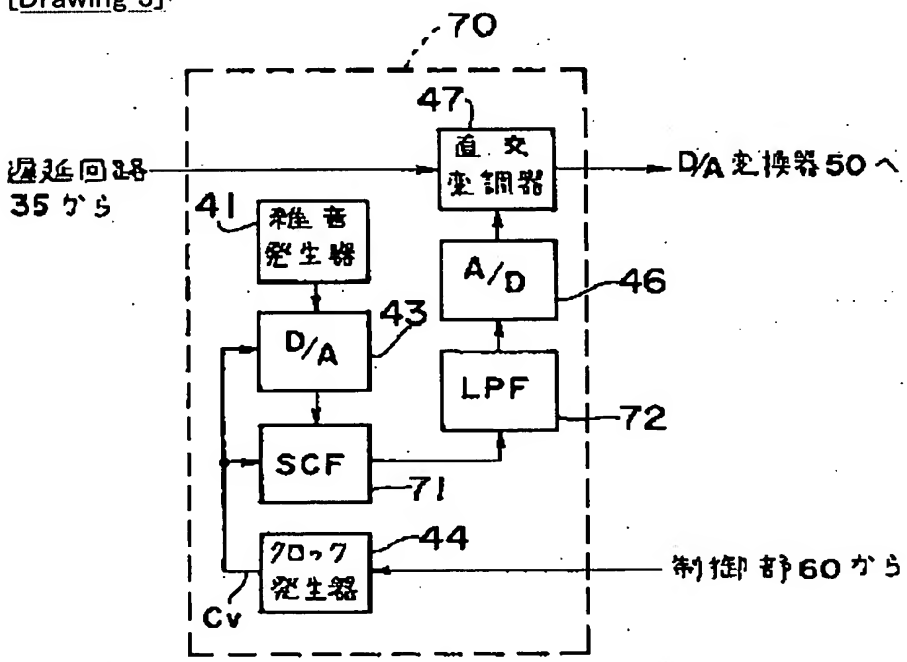
-- [procedure amendment]
[Filing Date] April 30, Heisei 10
[Procedure amendment 1]
[Document to be Amended] DRAWINGS
[Item(s) to be Amended] Complete diagram
[Method of Amendment] Modification
[Proposed Amendment]
[Drawing 1]



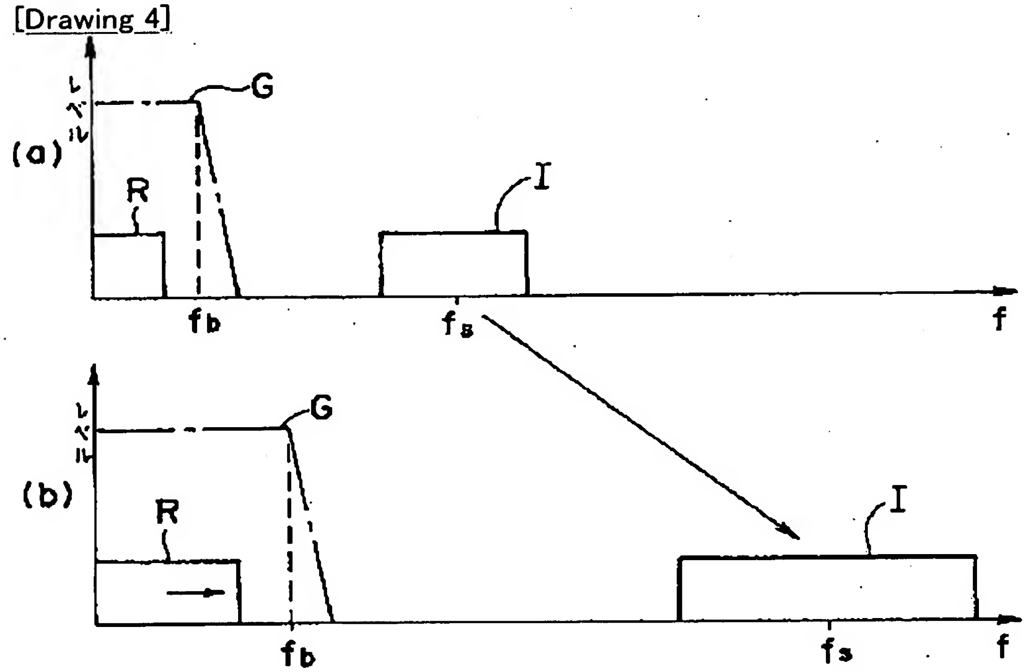
[Drawing 2]



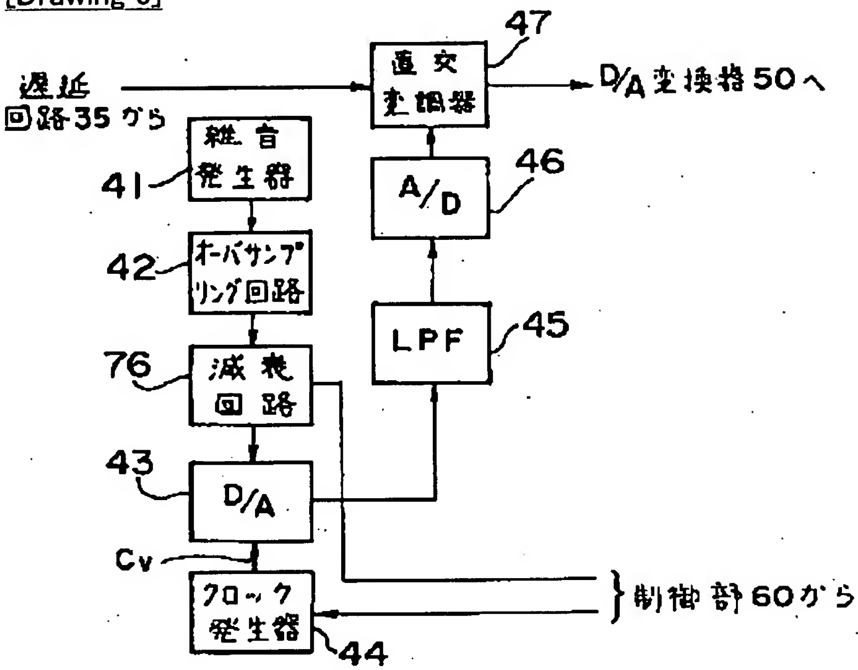
[Drawing 3]



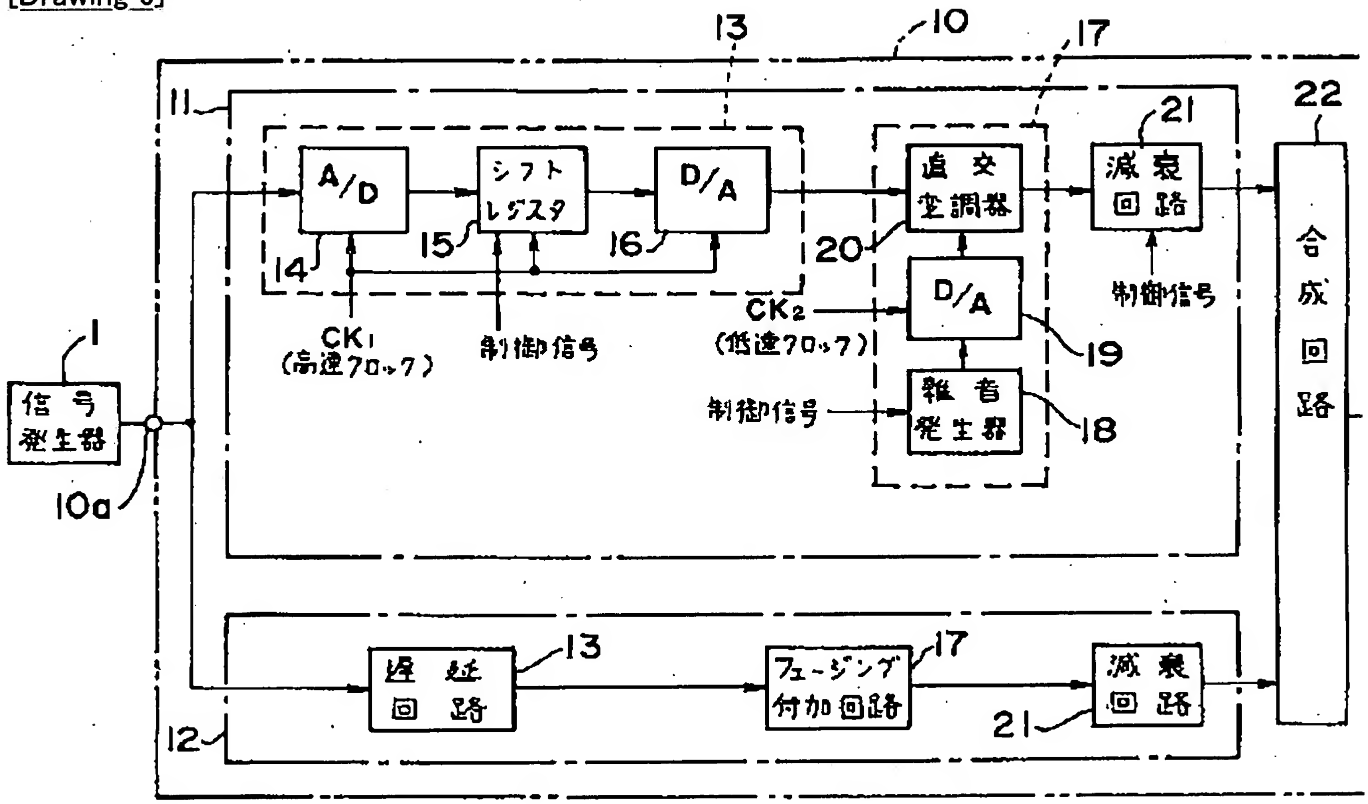
[Drawing 4]



[Drawing 5]



[Drawing 6]



[procedure amendment]

[Filing Date] July 9, Heisei 11
[Procedure amendment 1]
[Document to be Amended] Description
[Item(s) to be Amended] Whole sentence

[Method of Amendment] Modification
[Proposed Amendment]
[Document Name] Description
[Title of the Invention] Phasing simulator
[Claim(s)]
[Claim 1] In the phasing simulator output as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, and the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each,
Said phasing addition circuit
The noise generator which generates a digital noise signal (41),
An exaggerated sampling means to carry out exaggerated sampling processing of said noise signal, and to shift the image component of a noise signal to a high region side (42),
The frequency adjustable clock generation machine which outputs a clock signal (44),
The D/A converter which changes into an analog signal said noise signal by which exaggerated sampling processing was carried out synchronizing with the clock signal from said clock generation machine (43),
The low pass filter which removes said image component from the noise signal changed into the analog signal by said D/A converter (45),
The modulator which modulates the output signal of said delay circuit and gives phasing fluctuation and a doppler shift with the output signal of said low pass filter (47),
The phasing simulator which carries out adjustable control of the clock frequency of said clock generation machine, and is characterized by having the control means (60) which carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[Claim 2] Said attenuation circuit is a phasing simulator according to claim 1 characterized by giving attenuation indirectly to the output signal of said delay circuit by performing attenuation processing to the output signal of said exaggerated sampling means.
[Claim 3] In the phasing simulator output as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, and the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each,
Said phasing addition circuit
The noise generator which generates a digital noise signal (41),
The frequency adjustable clock generation machine which outputs a clock signal (44),
The D/A converter which changes said noise signal into an analog signal synchronizing with the clock signal from said clock generation machine (43),
The band adjustable filter from which the image component contained in the noise signal which the treble cut off frequency changed according to the frequency of the clock signal from said clock generation machine, and was outputted from said D/A converter is removed (71),
The modulator which modulates the output signal of said delay circuit and gives phasing fluctuation and a doppler shift with the output signal of said band adjustable filter (47),
The phasing simulator which carries out adjustable control of the clock frequency of said clock generation machine, and is characterized by having the control means (60) which carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[Claim 4] The phasing simulator according to claim 3 characterized by giving attenuation indirectly to the output signal of said delay circuit when said attenuation circuit performs attenuation processing to the noise signal outputted from said noise generator.
[Claim 5] It has the A/D converter (31) which changes said Sadanobu Tokoro number into a

digital signal,
Said delay circuit
Memory which can specify a write address and the read-out address independently (36),
A write-in means to make said memory memorize the digital signal which specified the write address to said memory in predetermined order, and was outputted from said A/D converter (37),
It has a read-out means (38) to read the digital signal which carried out sequential assignment of the read-out address to said memory, and was memorized by said memory, and to send out to said phasing addition circuit,
Said control means,
Claim 1 which the aforementioned read-out means carries out adjustable control of the read-out address specified as said memory, and is characterized by carrying out adjustable [of the time delay until reading appearance of the digital signal memorized by said memory is carried out] to arbitration, or a phasing simulator according to claim 2, 3, or 4.
[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention performs delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and in the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which performed these processings, in case delay characteristics and a phasing property are changed, it relates to the technique for making it not generate the hits of a signal.
[0002]
[Description of the Prior Art] It is necessary supposing many propagation paths to check actuation of wireless devices, such as a testing-machine machine for examining a terminal, a base station, or them, in the system which communicates by the electric wave.
[0003] Especially, in the case of a mobile station, the propagation property of a propagation path is sharply changed with time amount. The element of fluctuation of this propagation property is attenuation fluctuation by the travelling period difference of a multi-pass, phasing fluctuation, doppler shift fluctuation, a shelter, etc., in order to check actuation of a wireless device, needs to carry out delay processing, phasing attached processing, and attenuation processing to a predetermined signal, and needs to give the signal which performed these processings to a wireless device as a simulation propagation signal.
[0004] Drawing 6 shows the configuration of the phasing simulator 10 of the multi-pass mold generally used for such the object.
[0005] This phasing simulator 10 receives the Sadanobu Tokoro number (signal of the stable analog used for a communication link) outputted from the signal generator 1 through input terminal 10a, branches and inputs this into two propagation path simulation circuits 11 and 12.
[0006] The propagation path simulation circuits 11 and 12 are constituted by the attenuation circuit 21 which gives attenuation to the signal outputted from the delay circuit 13 delayed in a predetermined signal, the phasing addition circuit 17 which gives phasing fluctuation and a doppler shift to the signal outputted from the delay circuit 13, and the phasing addition circuit 17.
[0007] The delay circuit 13 is constituted by A/D converter 14 which changes an input signal into a digital signal, the shift register 15 which undergoes the output of A/D converter 14 and is made to generate fixed delay, and D/A converter 16 which changes the output from a shift register 15 into an analog signal, and changes the time delay over a Sadanobu Tokoro number by carrying out adjustable [of the number of stages of a shift register 15] with the control signal from the control section which is not illustrated.
[0008] The phasing addition circuit 17 is constituted by the noise generator 18, D/A converter 19, and the quadrature modulation machine 20, and with D/A converter 19, the digital white-noise signal outputted from a noise generator 18 is changed into the noise signal of an analog, and it outputs it to the quadrature modulation machine 20.
[0009] With the noise signal outputted from D/A converter 19, the quadrature modulation

machine 20 modulates the amplitude and phase of a predetermined signal, and gives phasing fluctuation and a doppler shift.
[0010] This phasing addition circuit 17 changes the amount of phasing fluctuation and the amount of doppler shifts to a predetermined signal by changing the program of a noise generator 18 with the control signal from a control section.
[0011] Moreover, an attenuation circuit 21 changes the magnitude of attenuation to the signal outputted from the phasing addition circuit 17 by the control signal from a control section.
[0012] Thus, the output of two constituted propagation path simulation circuits 11 and 12 is equivalent to the electric wave which was discharged from the same transmitter and passed through two different propagation paths, and can check actuation of the wireless device 2 by the actual busy condition by inputting into the wireless device 2 for assessment the composite signal which compounded both the output by the synthetic circuit 22 from output terminal 10b.
[0013]
[Problem(s) to be Solved by the Invention] However, by the above mentioned conventional phasing simulator, whenever it changes the amount of phasing fluctuation etc., the program of a noise generator will have to be changed, and the hits of a signal will occur between program modification.
[0014] Moreover, by the approach of changing the number of stages of a shift register like the above mentioned delay circuit, and carrying out adjustable [of the time delay], even if it changes the number of stages of a shift register for time delay modification, the delay signal meant promptly may not be outputted and trouble is in the check of a wireless device of operation.
[0015] This invention aims at offering the phasing simulator which solved these problems.
[0016]
[Means for Solving the Problem] In order to attain said object, the phasing simulator of claim 1 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates a digital noise signal (41), An exaggerated sampling means to carry out exaggerated sampling processing of said noise signal, and to shift the image component of a noise signal to a high region side (42), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes into an analog signal said noise signal by which exaggerated sampling processing was carried out synchronizing with the clock signal from said clock generation machine (43), The low pass filter which removes said image component from the noise signal changed into the analog signal by said D/A converter (45), The output signal of said delay circuit is modulated with the output signal of said low pass filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.
[0017] Moreover, the phasing simulator of claim 2 of this invention is characterized by said attenuation circuit giving attenuation indirectly to the output signal of said delay circuit by performing attenuation processing to the output signal of said exaggerated sampling means in a phasing simulator according to claim 1.
[0018] Moreover, the phasing simulator of claim 3 of this invention The delay circuit which performs delay processing to the inputted Sadanobu Tokoro number, and the phasing addition circuit which adds phasing fluctuation in response to the output of said delay circuit, In the phasing simulator outputted as a simulation propagation signal which spread the propagation path from which a propagation property changes the signal which has the attenuation circuit which carries out attenuation processing of the output of said phasing addition circuit, and performed these processings of each The noise generator with which said phasing addition circuit generates

a digital noise signal (41), The frequency adjustable clock generation machine (44) which outputs a clock signal, and the D/A converter which changes said noise signal into an analog signal synchronizing with the clock signal from said clock generation machine (43), The band adjustable filter from which the image component contained in the noise signal which the treble cut off frequency changed according to the frequency of the clock signal from said clock generation machine, and was outputted from said D/A converter is removed (71), The output signal of said delay circuit is modulated with the output signal of said band adjustable filter. It has the control means (60) which carries out adjustable control of the clock frequency of the modulator (47) which gives phasing fluctuation and a doppler shift, and said clock generation machine, and carries out adjustable [of the amount of phasing fluctuation to an output signal and the amount of doppler shifts of said delay circuit] to arbitration.

[0019] Moreover, in a phasing simulator according to claim 3, the phasing simulator of claim 4 of this invention is characterized by giving attenuation indirectly to the output signal of said delay circuit, when said attenuation circuit performs attenuation processing to the noise signal outputted from said noise generator.

[0020] Moreover, the phasing simulator of claim 5 of this invention In claim 1 or a phasing simulator according to claim 2, 3, or 4 The memory as which it has the A/D converter (31) which changes said Sadanobu Tokoro number into a digital signal, and said delay circuit can specify a write address and the read-out address independently (36), A write-in means to make said memory memorize the digital signal which specified the write address to said memory in predetermined order, and was outputted from said A/D converter (37), It has a read-out means (38) to read the digital signal which carried out sequential assignment of the read-out address to said memory, and was memorized by said memory, and to send out to said phasing addition circuit. The aforementioned read-out means carries out adjustable control of the read-out address specified as said memory, and said control means is characterized by carrying out adjustable [of the time delay until reading appearance of the digital signal memorized by said memory is carried out] to arbitration.

[0021]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of this invention is explained based on a drawing. Drawing 1 shows the configuration of the phasing simulator 30 of the two pass mold of 1 operation gestalt of this invention.

[0022] In addition, this invention operates also by the phasing simulator of an one-pass mold. In the case of a two pass mold, in the case of an one-pass mold, it becomes with the trial of only the direct propagation root to the trial of the 2 roots of the direct propagation root for example, between stations and the root of a reflected wave being possible. 2 propagation root of a reflected wave other than a reflected wave as a two pass mold can also be examined. Moreover, pass is increased with three pass, four pass, and --, and it can also examine. Since all of a principle are the same, a two pass mold explains here.

[0023] In drawing 1 , the Sadanobu Tokoro number outputted from a signal generator 1 is inputted into A/D converter 31 through input terminal 30a of the phasing simulator 30.

[0024] A/D converter 31 samples a predetermined signal with the period which synchronizes with a clock signal Ck, and changes it into a digital signal.

[0025] The Sadanobu Tokoro number changed into the digital signal branches, and is inputted into two propagation path simulation circuits 32 and 33 by A/D converter 31.

[0026] The propagation path simulation circuits 32 and 33 are the same configurations, and are constituted by the delay circuit 35, the phasing addition circuit 40, D/A converter 50, and the attenuation circuit 51, respectively.

[0027] A delay circuit 35 constitutes the delay circuit of this operation gestalt with the control section 60 mentioned later, and is constituted by memory 36, the write-in circuit 37, and the read-out circuit 38. Memory 36 can specify a write address and the read-out address independently, and is formed by the dual port RAM which has independent input/output port.

[0028] The write-in circuit 37 specifies the write address Aw to memory 36 in predetermined order synchronizing with a clock signal Ck, and makes memory 36 memorize the digital signal outputted from A/D converter 31.

[0029] The read-out circuit 38 reads the digital signal which carried out sequential assignment of the read-out address Ar to memory synchronizing with the clock signal Ck, and was memorized by memory 36.
[0030] Therefore, only the time amount which multiplied by the period of a clock signal Ck is behind [difference deltaA of a write address Aw and the read-out address Ar] in the digital signal written in memory 36, and reading appearance is carried out to it. In addition, according to the delay control signal from a control section 60 mentioned later, the read-out circuit 38 carries out adjustable [of the read-out address Ar] so that deltaA may change.
[0031] The phasing addition circuit 40 inputs into the exaggerated sampling circuit 42 the digital white-noise signal outputted from the noise generator 41 which constitutes the phasing addition circuit of this operation gestalt with the control section 60 mentioned later, and was constituted by DSP.
[0032] If the noise signal sequences outputted from the noise generator 41 are {N1, N2, --, Nk, -- }, the exaggerated sampling circuit 42 This like {N1, 0, --, 0N2, 0, --, 0, --, Nk, 0, --, 0, --} Only an image component is shifted to a high region by interpolating between each signal by zero data of two or more (M-1) individuals, and making a digital filter pass this, without changing the signal component of a noise signal itself. Thus, the method which interpolates and filters between signals by M-1 data [zero] is called exaggerated sampling M times.
[0033] It is [as opposed to / when are explained in more detail and D/A conversion of the noise signal outputted from the noise generator 41 is carried out at the rate of the frequency fs of the clock generation machine 44, without carrying out exaggerated sampling processing, as it is shown in drawing 2 / the fundamental component R of a noise signal] the image component I1 with the nearest frequency. It generates focusing on a frequency fs. Therefore, this image component I1 The low pass filter for removing is needed.
[0034] Like the property F of drawing 2 , the treble cut off frequency fa of this low pass filter is usually the image component I1, when maximum of a frequency fs was set to fsm, the band of the fundamental component R of a noise signal it is whose frequency at the fsm time, and the treble cut off frequency fa of a filter are set as fsm/2, adjustable [of the frequency fs] is carried out and the band of a fundamental component R is narrowed, since [of a frequency fs] about 1/was set as 2. A low pass filter will be passed.
[0035] On the other hand, when exaggerated sampling processing is performed M times to the noise signal outputted from the noise generator 41 like this operation gestalt, it is [as opposed to / as shown in drawing 2 / the fundamental component R of a noise signal] the image component I2 with the nearest frequency. It generates focusing on frequency M-fs. Also after this has fixed the treble cut off frequency of the low pass filter 45 mentioned later, ranging from fa/2 to fsm/2, it can carry out adjustable [of the band of the fundamental component R of a noise signal] mostly by carrying out adjustable [of the frequency fs].
[0036] Thus, the noise signal by which exaggerated sampling processing was carried out is changed into an analog signal by D/A converter 43. D/A converter 43 changes a noise signal into an analog signal synchronizing with clock signal Cv from the clock generation machine 44, and outputs it to a low pass filter 45.
[0037] The clock generation machine 44 carries out adjustable [of the frequency of clock signal Cv] according to the noise control signal from a control section 60 mentioned later, carries out adjustable [of the band of the fundamental component of a noise signal], and changes the wave of a noise signal.
[0038] The output signal of a low pass filter 45 is changed into a digital signal by A/D converter 46, and is outputted to the quadrature modulation machine 47 by it. In addition, A/D converter 46 performs digital conversion synchronizing with a clock signal Ck.
[0039] The quadrature modulation machine 47 modulates the digital signal by which reading appearance was carried out from the memory 36 of a delay circuit 35 with the digital noise signal outputted from A/D converter 46, and adds phasing fluctuation and a doppler shift.
[0040] The signal outputted from the quadrature modulation machine 47 is changed into an analog signal by D/A converter 50, and is inputted into an attenuation circuit 51.
[0041] An attenuation circuit 51 changes the magnitude of attenuation to the signal outputted

from the quadrature modulation machine 47 according to the attenuation control signal from a control section 60.
[0042] The signal outputted from each attenuation circuit 51 of the propagation path simulation circuits 32 and 33 is inputted and compounded by the synthetic circuit 52, and the composite signal is outputted to the wireless device 2 for assessment from output terminal 30b.
[0043] A control section 60 outputs the input signal when receiving moving [according to the fluctuation pattern set up beforehand, changed continuously the delay control signal, noise control signal, and attenuation control signal over the delay circuit 35, the phasing addition circuit 40, and attenuation circuit 51 of the propagation path simulation circuits 32 and 33, for example,] the electric wave from a base station, when the wireless device 2 for assessment is a mobile station, and the composite signal changed similarly to the wireless device 2.
[0044] Thus, delay processing of the phasing simulator 30 of an operation gestalt memorizes the Sadanobu Tokoro number changed into the digital signal by A/D converter 31 in order of the address in the memory 36 which can specify a write address and the read-out address independently, carries out adjustable [of the difference of the read-out address to a write address], and is carrying out adjustable [of the time delay of a signal] while it reads this one by one in the condition that there is an address difference.
[0045] For this reason, in case a time delay is changed, the exact time delay corresponding to the difference of the address can be given promptly.
[0046] Moreover, phasing attached processing of the phasing simulator 30 After carrying out exaggerated sampling processing of the noise signal of band immobilization to the fixed sampling rate outputted from the noise generator 41 by DSP Carry out D/A conversion, change into an analog signal, the low pass filter 45 of frequency immobilization removes an image component from this signal, and it inputs into the quadrature modulation machine 47. Phasing fluctuation and a doppler shift are given to the signal outputted from the delay circuit 35, adjustable [of the clock frequency to D/A converter 43] is carried out, adjustable [of the band of a noise signal] is carried out, and the amount of phasing fluctuation and the amount of doppler shifts are fluctuated.
[0047] For this reason, a noise signal with a high precision is acquired, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing the program of DSP, and the hits of a signal do not occur.
[0048]
[The gestalt of other operations] Although the image frequency of the noise signal generated by performing exaggerated sampling processing to a noise signal at the time of D/A conversion was shifted to the high region side and the low pass filter of frequency immobilization had removed the image frequency in phasing attached processing of said operation gestalt The noise signal outputted from the noise generator 41 is changed into the noise signal of an analog with D/A converter 43 like the phasing addition circuit 70 shown in drawing 3 . You may make it a switched capacitor filter (for it to be hereafter described as SCF) 71 remove the image component contained in this noise signal.
[0049] In addition, the low pass filter (LPF) 72 prepared in the latter part of SCF71 is for removing a clock signal Cv component from the output of SCF71.
[0050] SCF71 is a band adjustable filter element which performs the band limit to an input signal with the cut-off frequency according to the frequency of clock signal Cv, and when it uses as a low pass filter, if the frequency of clock signal Cv becomes high, according to it, a treble cut off frequency will shift it to the higher one.
[0051] In a certain clock frequency therefore, like the property G of (a) of drawing 4 If the treble cut off frequency fb of SCF71 is set as the frequency slightly higher than the band of the fundamental component R of a noise signal As shown in (b) of drawing 4 , when it carries out adjustable [of the frequency of clock signal Cv], the treble cut off frequency fb of SCF71 also changes in the same direction. The amount of phasing fluctuation and the amount of doppler shifts can be changed without being able to remove the image component I of a noise signal, being able to pass the fundamental component R, and generating the hits to a signal.

[0052] In addition, although SCF71 is used as a band adjustable filter, if it can carry out adjustable [of the treble cut off frequency] according to the frequency of the clock signal of D/A converter 43, other band adjustable filters can also be used here.
[0053] Moreover, although this invention was applied to the phasing simulator of the two pass mold which has two propagation path simulation circuits with said operation gestalt, the phasing simulator and propagation path simulation circuit of 3 or more ****s can apply this invention also like the phasing simulator of only one one-pass mold.
[0054] Moreover, although it is made to perform attenuation processing directly with said operation gestalt to the signal which delay processing and phasing attached processing constituted For example, as shown in drawing 5 , exaggerated sampling processing of the noise signal outputted from the noise generator 41 is carried out by the exaggerated sampling circuit 42. You may constitute so that the noise signal by which exaggerated sampling processing was carried out may be inputted into the attenuation circuit 76 of a digital mold, attenuation processing may be performed and the signal which carried out attenuation processing may be changed into an analog signal with D/A converter 43.
[0055] In addition, when an attenuation circuit 76 is formed between a noise generator 41 and the exaggerated sampling circuit 42, an attenuation circuit will operate synchronizing with the clock of D/A converter 43, but like drawing 5 , when an attenuation circuit 76 is formed between the exaggerated sampling circuit 42 and D/A converter 43, attenuation control and adjustable control of the clock of D/A converter 43 can be performed independently, and attenuation processing can be performed without delay.
[0056] In addition, when an attenuation circuit is prepared in a phasing addition circuit like drawing 5 , the output of D/A converter 50 is compounded by the synthetic circuit 52, and it gives to the wireless device 2.
[0057]
[Effect of the Invention] As explained above, by the phasing simulator of claim 1 of this invention After carrying out exaggerated sampling processing of the digital noise signal outputted from the noise generator While modulating a Sadanobu Tokoro number with the noise signal which carried out D/A conversion, changed into the analog signal, removed the image component from this signal with the low pass filter of frequency immobilization, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are given to the predetermined signal.
[0057] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.
[0058] moreover, by the phasing simulator of claim 3 of this invention Carry out D/A conversion of the digital noise signal outputted from the noise generator, and it changes into an analog signal. While modulating a Sadanobu Tokoro number with the noise signal which removed the image component from this signal with the band adjustable filter, and removed this image component Adjustable [of the clock frequency to a D/A converter] was carried out, adjustable [of the band of a noise signal] was carried out, and phasing fluctuation and a doppler shift are given to the predetermined signal.
[0059] For this reason, phasing fluctuation and a doppler shift with a high precision can be given, moreover adjustable [of the band of a noise signal] can be carried out, without changing a program, and the hits of a signal do not occur.
[0060] Moreover, by the phasing simulator of claim 5 of this invention, in the above-mentioned phasing simulator, the Sadanobu Tokoro number changed into the digital signal by the A/D converter is memorized in order of the address in the memory which can specify a write address and the read-out address independently, and while reading this one by one in the condition that there is an address difference, adjustable [of the difference of the read-out address to a write address] is carried out, and it is carrying out adjustable [of the time delay of a signal].
[0061] For this reason, while giving phasing fluctuation and a doppler shift with a high precision, in case a time delay is changed, the exact time delay corresponding to an address difference can

be given promptly.
[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the configuration of 1 operation gestalt of this invention
[Drawing 2] Drawing for explaining actuation of 1 operation gestalt
[Drawing 3] The block diagram showing the configuration of other operation gestalten of this invention
[Drawing 4] Drawing for explaining actuation of other operation gestalten
[Drawing 5] The block diagram showing the configuration of other operation gestalten of this invention
[Drawing 6] The block diagram showing the configuration of equipment conventionally
[Description of Notations]
30 Phasing Simulator
31 A/D Converter
32 33 Propagation path simulation circuit
35 Delay Circuit
36 Memory
37 Write-in Circuit
38 Read-out Circuit
40 Phasing Addition Circuit
41 Noise Generator
42 Exaggerated Sampling Circuit
43 D/A Converter
44 Clock Generation Machine
45 Low Pass Filter
46 A/D Converter
47 Quadrature Modulation Machine
50 D/A Converter
51 Attenuation Circuit
52 Synthetic Circuit
60 Control Section

[Translation done.]